1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
3	0003501996	ENGINEERING RELEASED	2014-12-09

J117 MLB

LAST_MODIFIED=Thu Sep 18 13:37:48 2014
LAST_MODIFICATION=Thu Sep 18 13:37:48 2014

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DRAWING
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ABBREV=DRAWING
LAST_MODIFIED=Thu Sep 18 13:37:48 2014

DRAWING TITLE: SCHEM,MLB,J117

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DRAWING NUMBER: 051-00081 | SIZE: D
REVISION: 3.0.0
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DRAWING

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-00081	1	SCH,MLB,J117	SCH	CRITICAL	
820-00034	1	PCBF,MLB,J117	PCB	CRITICAL	
685-00013	1	PCBA,MLB,J117,COMMON PARTS	CMNPTS		MLB_CMNPTS

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00016	PCBA,MLB,DEV,J117	DEVELOPMENT,J117_DEVEL
939-00158	PCBA,MLB,DEV,J117,CPU_INT	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,DDR3:HYNIX_8GB_1866,SSD:Y
639-00910	PCBA,MLB,J117,HY_8GB_29NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_1866,SSD:N
639-00911	PCBA,MLB,J117,EL_8GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_1866,SSD:N
639-00912	PCBA,MLB,J117,SA_8GB_23NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:SAMSUNG_8GB_1866,SSD:N
639-00913	PCBA,MLB,J117,EL_16GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_16GB_1866,SSD:N
639-00914	PCBA,MLB,J117,HY_16GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_16GB_1866,SSD:N
639-00713	PCBA,MLB,J117,HY_8GB_29NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_1866,SSD:Y
639-00714	PCBA,MLB,J117,EL_8GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_1866,SSD:Y
639-00715	PCBA,MLB,J117,SA_8GB_23NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:SAMSUNG_8GB_1866,SSD:Y
639-00716	PCBA,MLB,J117,EL_16GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_16GB_1866,SSD:Y
639-00717	PCBA,MLB,J117,HY_16GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_16GB_1866,SSD:Y
685-00013	PCBA,MLB,J117,COMMON PARTS	J117_COMMON

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S00011	377S0155		ALL	USB3 diodes
377S0184	377S0155		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0479	197S0478		ALL	12 MHz Cam. Xtal
197S0486	197S0478		ALL	12 MHz Cam. Xtal
107S0251	107S0249		ALL	Sense resistor
197S0481	197S0480		ALL	25MHz Xtal
197S0343	197S0480		ALL	25MHz Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
378S0391	378S0390		ALL	Debug LEDs
341S00016	341S3912		ALL	ENET ROM,ADESTO,V1.15
138S0747	138S0773		ALL	1uF,X6S,402
197S0542	197S0544		ALL	24 MHz PCH XTal
197S0545	197S0544		ALL	24 MHz PCH XTal
197S0369	197S0392		ALL	32 KHz PCH Xtal
197S0399	197S0392		ALL	32 KHz PCH Xtal
376S0572	376S0659		ALL	Single P-Ch FET
376S0972	376S00075		ALL	Single N-Ch FET
132S00012	132S0401		ALL	0.22uF,X7R,0402
138S00012	138S0771		ALL	1uF,X6S,0402
138S1103	138S0719		ALL	4.7uF,X5R,0402
155S0830	155S0316		ALL	FER BD,600 OHM,0.5A,0603
155S00076	155S0546		ALL	FER BD,600 OHM,300MA,402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1089	376S1128		ALL	Single N-Ch FET
155S0660	155S0513		ALL	220HM EMI BEAD
155S0694	155S0387		ALL	470OHM EMI BEAD
127S0164	127S0162		ALL	1UF 25V TANT
376S00074	376S0855		ALL	Dual N-Ch FET
376S1129	376S0855		ALL	Dual N-Ch FET
376S00074	376S0855	SSD:Y	ALL	Dual N-Ch FET
376S1129	376S0855	SSD:Y	ALL	Dual N-Ch FET
311S0649	311S0541		ALL	Single AND Gate
107S0375	107S00039		ALL	DDR Sense Res
107S00011	107S0372		ALL	CPU VR Sense Res
353S3814	353S3812		ALL	TBT mux
353S4376	353S3384		ALL	HDD OOBv1 comparator
311S00014	311S0515		ALL	TBT JTAG ISOLATION BUFFER
311S00013	311S0508		ALL	Single Buffer Driver OD
371S00019	371S0463		ALL	Rohm Schottky Barrier Diode
376S00037	376S1193		ALL	30V,64A,Single N-Channel FET
376S00036	376S1194		ALL	30V,52A,Single N-channel FET
138S0746	138S0705		ALL	CAP,CER,X5R,10uF,20%,10V,402
152S1757	152S1821		ALL	IND,0.4uH,23A
138S00013	138S0772		ALL	CAP,CER,2.2UF,20%,10V,X6S,402
371S00017	371S0749		ALL	DIODE,SCHOTTKY,30V,1A,SOD-323

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00065	08	CPU,BDW-ULT,2+GT3
338S1247	02	TBT,Falcon Ridge-4c
335S00006	07	IC,SERIAL FLASH,Quad-IO
333S0784	07	32Gb,25nm LPDDR3-1866
333S0786	07	16Gb,29nm LPDDR3-1866
333S0790	07	32Gb,25nm LPDDR3-1866
333S0792	07	16Gb,25nm LPDDR3-1866
333S00004	07	16Gb,23nm LPDDR3-1866

BOM Groups

BOM GROUP	BOM OPTIONS
J117_COMMON	COMMON,ALTERNATE,J117_PROGPARTS,SMCREG:SUP,XDP,SMBUS1:ISOL,USB_OC_ISO:Y,RTCRST:Y,AUDIO_DP_SNS:N
J117_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
J117_DEVEL	XDP_CONN,TEMPSNSDEV,SAMCONN

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00101	1	IC,CPU,BDW-ULT,QH3Y,E8,f0-B2,2/2,1.4,15W,.95,1168	U0500	CRITICAL	CPU:ULT
998-7866	1	INTERPOSER,BGA1168,SINGLE SIDE	U0500	CRITICAL	CPU:SOCKET

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00158	1	IC,EFI,V0108,J117	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,SERIAL FLASH,64MBIT,3V,RP,WSON,QE=1	U5210	CRITICAL	BOOTROM:BLANK
341S00110	1	IC,SMC-B1,EXTERNAL,V2.24A19,POC,J117	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/50MIPS,MCU,157BGA	U5000	CRITICAL	SMC:BLANK
341S3778	1	IC,CAMERA,FLASH,V7229,J16	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00154	1	IC,EPROM,T29,FALCON RIDGE,V27.1,J117	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,FLASH,SPI,4MBIT,50MHZ	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET SPI ROM,NVMONYX,V1.15,216/2160/217	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_8GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,HYNIX_8GB_1600
DDR3:HYNIX_16GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,RAMCFG4:L,HYNIX_16GB_1600
DDR3:HYNIX_8GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,HYNIX_8GB_1866
DDR3:HYNIX_16GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,RAMCFG4:H,HYNIX_16GB_1866
DDR3:ELPIDA_8GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,ELPIDA_8GB_1600
DDR3:ELPIDA_16GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,RAMCFG4:L,ELPIDA_16GB_1600
DDR3:ELPIDA_8GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,ELPIDA_8GB_1866
DDR3:ELPIDA_16GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,RAMCFG4:H,ELPIDA_16GB_1866
DDR3:SAMSUNG_8GB_1600	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,SAMSUNG_8GB_1600
DDR3:SAMSUNG_8GB_1866	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,SAMSUNG_8GB_1866

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	0	1
N/A	1	0
ELPIDA	1	1

SIZE	CFG 2
8GB	0
16GB	1

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1600
333S0784	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1866
333S0785	4	IC,SDRAM,29nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1600
333S0786	4	IC,SDRAM,29nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1866
333S0789	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1600
333S0790	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1866
333S0791	4	IC,SDRAM,25nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1600
333S0792	4	IC,SDRAM,25nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1866
333S00003	4	IC,SDRAM,23nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1600
333S00004	4	IC,SDRAM,23nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1866

DIE REV	CFG 3
A	0
B	1

SPEED	CFG 4
1600	0
1866	1

SYNC_MASTER=J117_TONY SYNC_DATE=05/05/2014

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BOM Configuration

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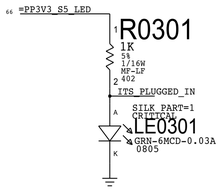
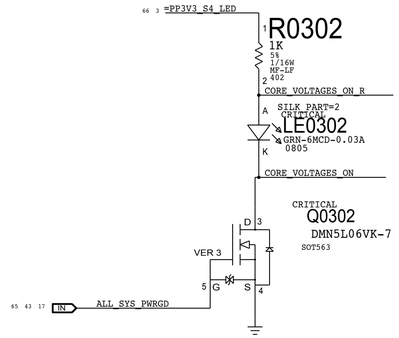
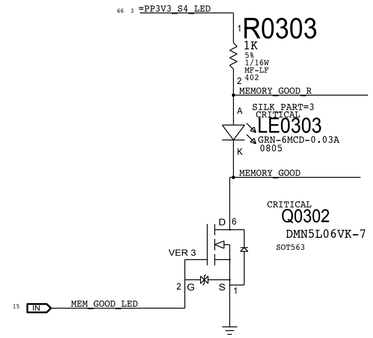
S5 Led



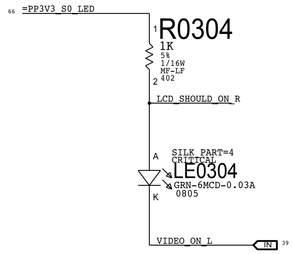
ALL_SYS_PWRGD Led



MEM_GOOD Led



VIDEO ON Led



SYNC_MASTER=J70_GAREN SYNC_DATE=10/22/2013

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DEBUG LEDS

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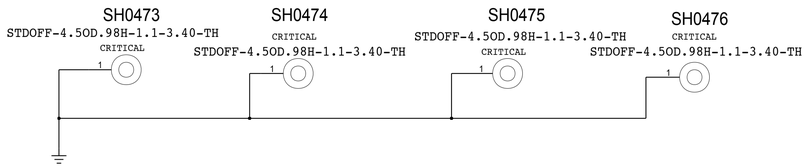
CPU HEATSINK MOUNTING FEATURES

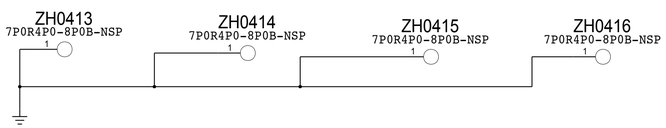


HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

Rear Cover

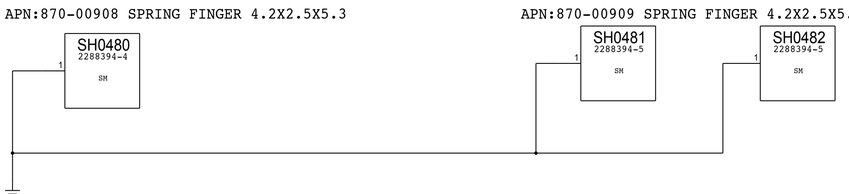
APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



J117 SPRINGS

APN:870-00908 SPRING FINGER 4.2X2.5X5.3

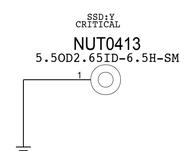
APN:870-00909 SPRING FINGER 4.2X2.5X5.81



WIRELESS CARD MTG HOLES

APN:998-01406 (Plated holes, 2.1mm inner diameter, 4.3mm top pad, 5.1mm bottom pad)

SSD STANDOFF
APN: 860-00198



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
Holes/PD parts

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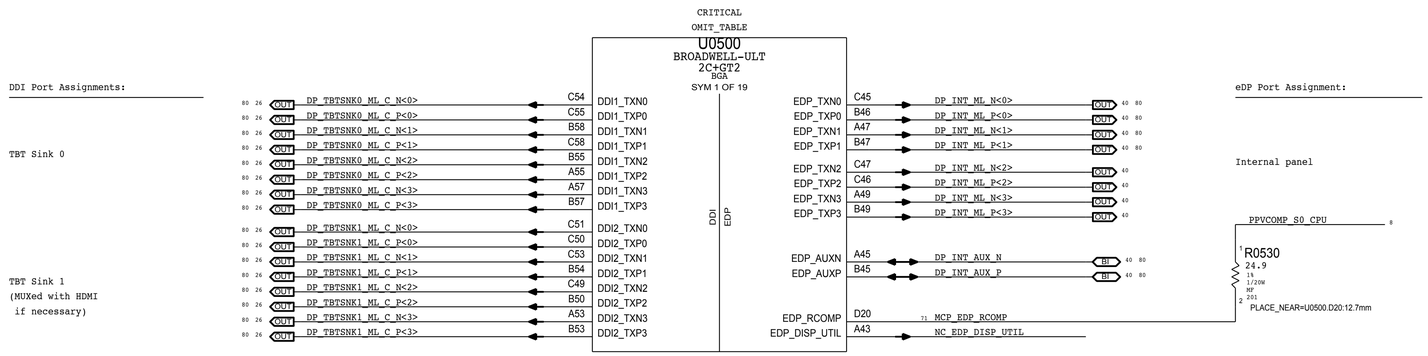
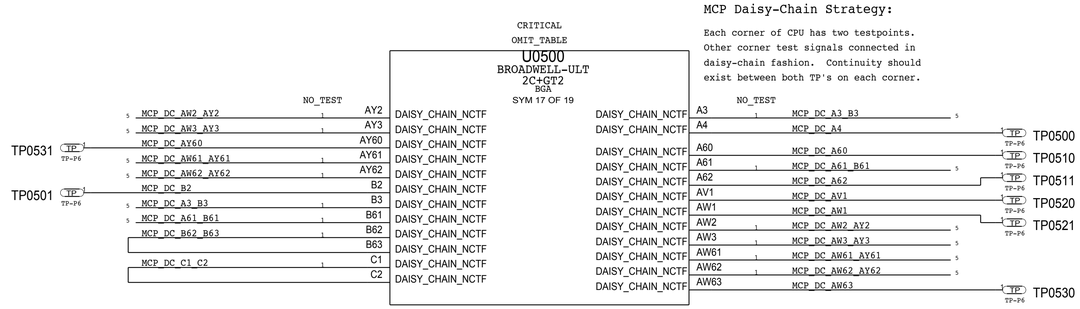
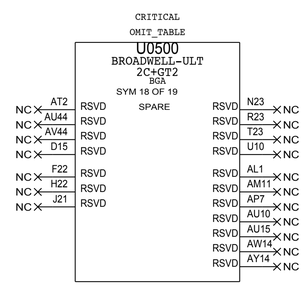




MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.



SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

CPU GFX/NCTF/RSVD

Apple Inc.

DRAWING NUMBER 051-00081

SIZE D

REVISION 3.0.0

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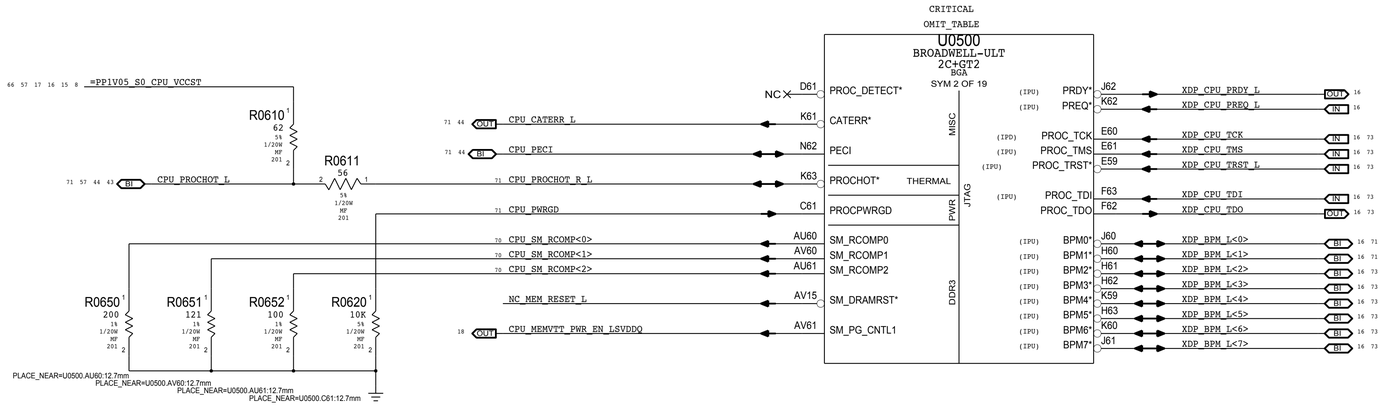
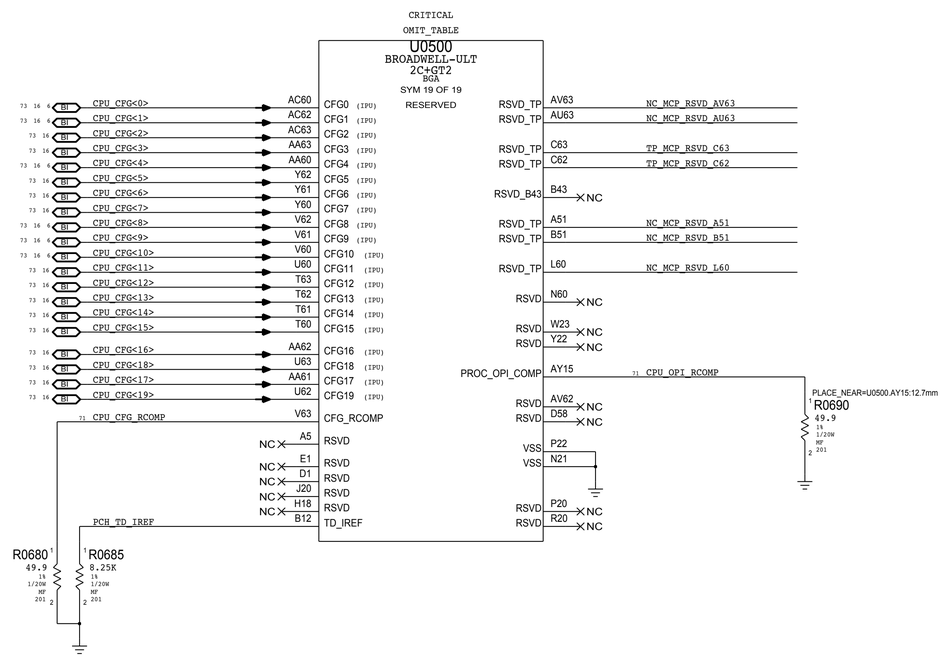
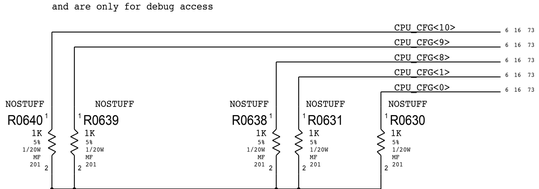


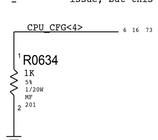


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE	
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID	
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED	
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED	
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE	
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK	

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



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CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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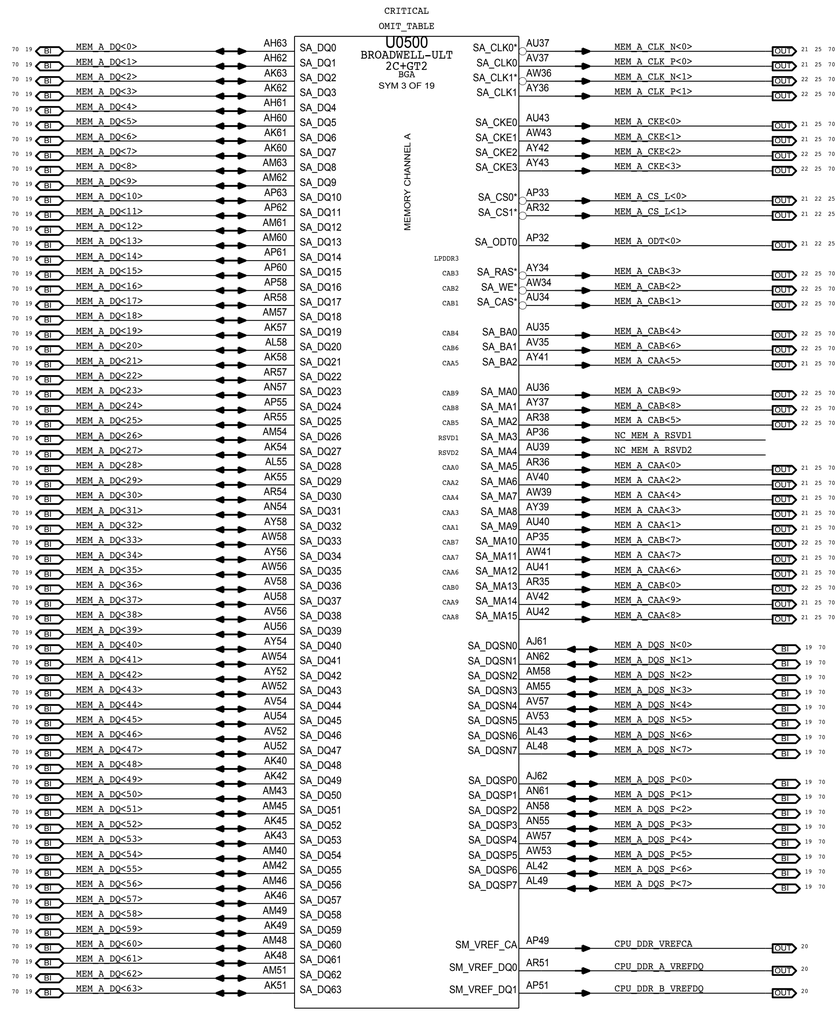

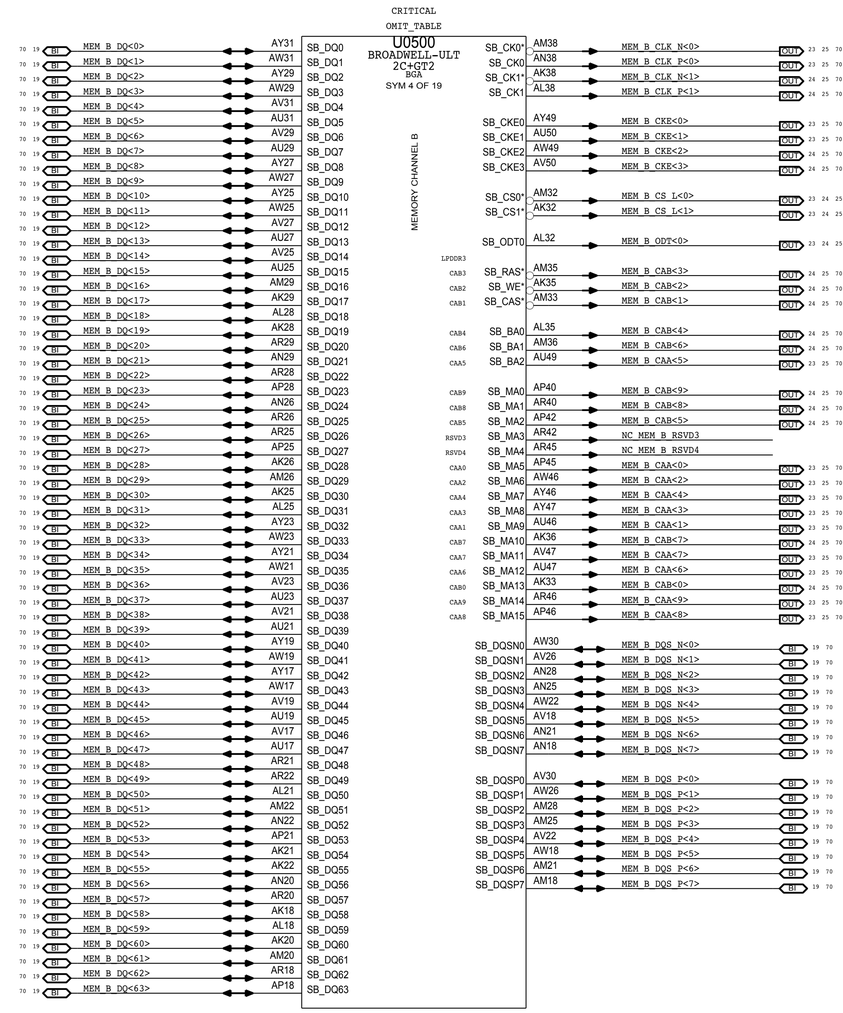

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CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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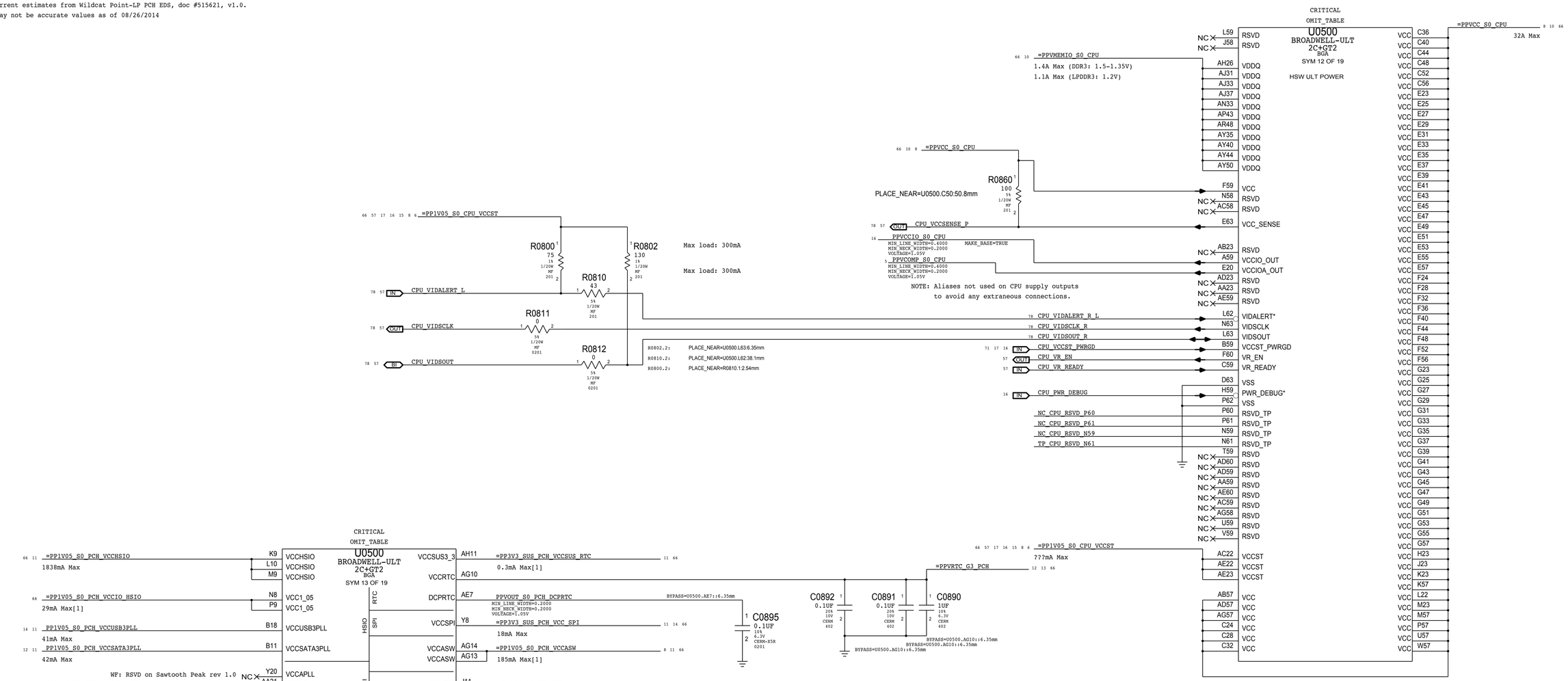
BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol 1, doc #514405, v1.5.
WPT-LP current estimates from Wildcat Point-LP PCH EDS, doc #515621, v1.0.
Numbers may not be accurate values as of 08/26/2014



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CPU/PCH POWER

Apple Inc.

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CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS	VSS	V58
G5	VSS	VSS	AH46
G6	VSS	VSS	V23
G8	VSS	VSS	E62
H13	VSS	VSS_SENSE	AH16

CPU_VCCSENSE_N — OUT — 57 78

R0960
100
5%
1/20W
MF
201
1 — 2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER 051-00081
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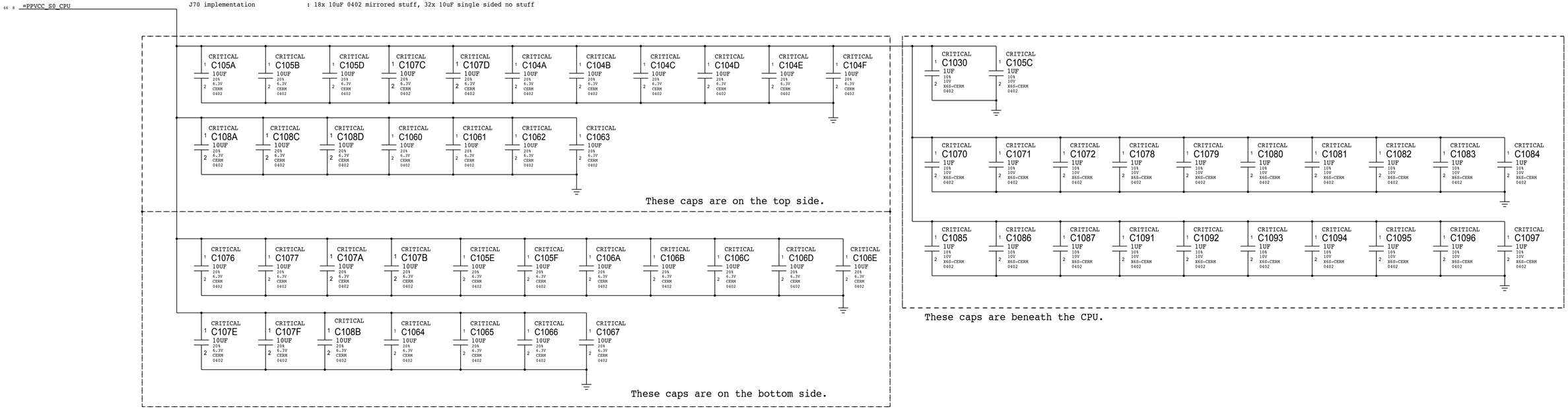
All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

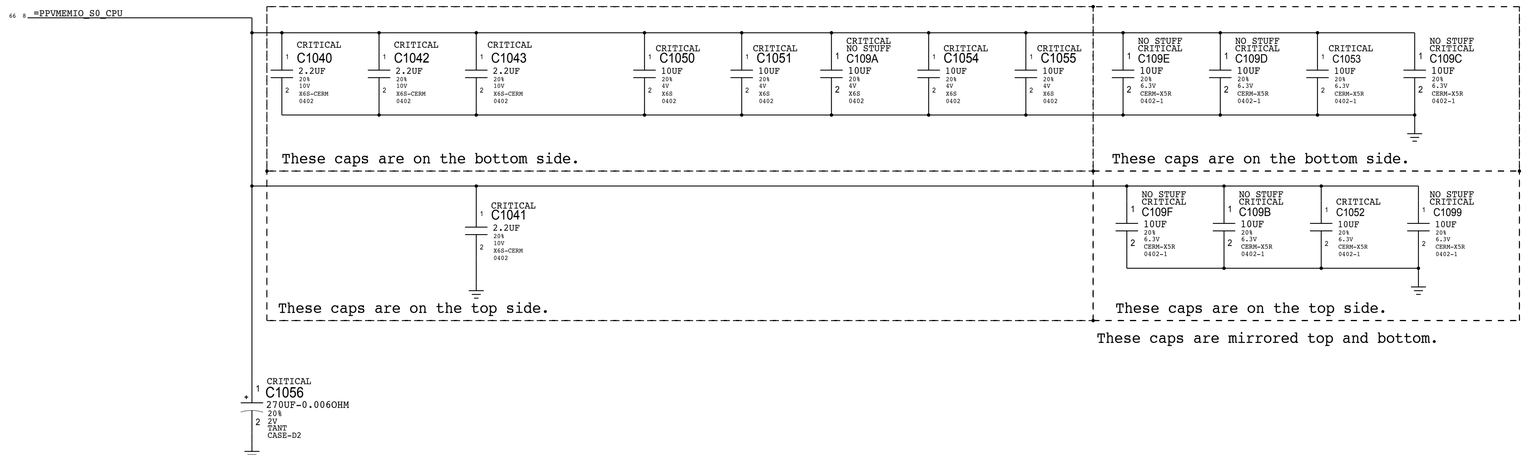
CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff
J70 implementation : 18x 10uF 0402 mirrored stuff, 32x 10uF single sided no stuff



CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 6x 10uF no stuff, 1x 270 uF Bulk



SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: CPU Decoupling

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DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
=PP3V3_S5_PCH_VCCDSW
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
=PP3V3_S0_PCH_VCC3_3_GPIO
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8::12.7mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
=PP1V05_S0_PCH_VCCASW
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9::12.7mm
BYPASS=U0500.AE9::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
=PP1V05_S0_PCH_VCCIO_USB2
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
=PP3V3_SUS_PCH_VCC_SPI
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
=PP3V3_S0_PCH_VCCTS
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14::6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
=PP1V05_S0_PCH_VCC
C1255 10UF 20% 6.3V CERM-X5R 0402-1
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11::12.7mm
BYPASS=U0500.J11::6.35mm
BYPASS=U0500.AE8::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
=PP1V05_S0_PCH_VCCCLK
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17::6.35mm
BYPASS=U0500.R21::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
=PP3V3_SUS_PCH_VCCSUS_GPIO
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9::12.7mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
=PP1V05_S0_PCH_VCCHSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9::6.35mm
BYPASS=U0500.L10::6.35mm
BYPASS=U0500.M9::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
=PP3V3_SUS_PCH_VCCSUS_RTC
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11::6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V SDIO PWR)
=PP3V3_S0_PCH_VCCSDIO
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8::6.35mm

=PP1V05_S0_PCH_PLLFILTERS
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::6.35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
C1272 1UF 10% 10V X5R 402-1
31mA Max

PCH VCCSUSHDA BYPASS
(PCH 1.5V HDA PWR)
=PP1V5_S0_PCH_VCCSUSHDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14::6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::6.35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
C1277 1UF 10% 10V X5R 402-1
??mA Max

R1280 0 5% 1/16W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
NO STUFF
C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF
C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402-1
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
57mA Max

=PP1V05_S0_PCH_VCCPLL_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF
C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402-1
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
42mA Max

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF
C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402-1
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::6.35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
41mA Max

WPT-LP current estimates from Wildcat Point-LP PCH EDS, doc #515621, v1.0
These numbers may not be accurate as of 08/26/2014

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014
PAGE TITLE
PCH Decoupling
Apple Inc.
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REVISION 3.0.0
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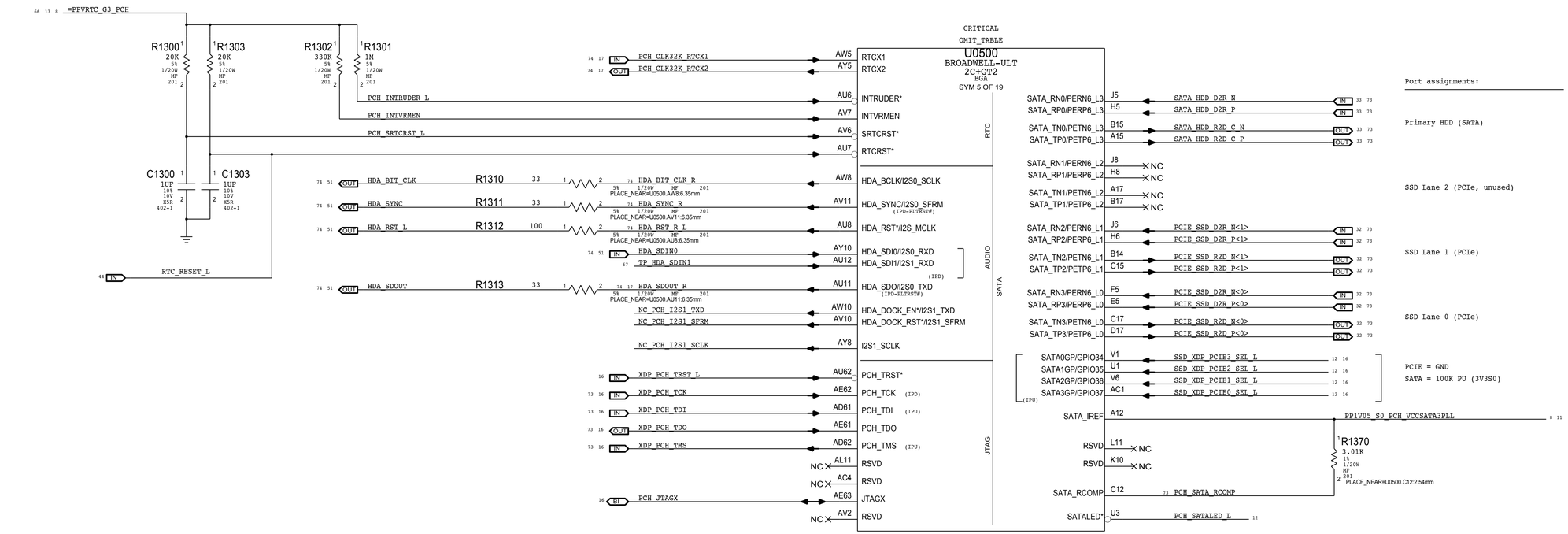
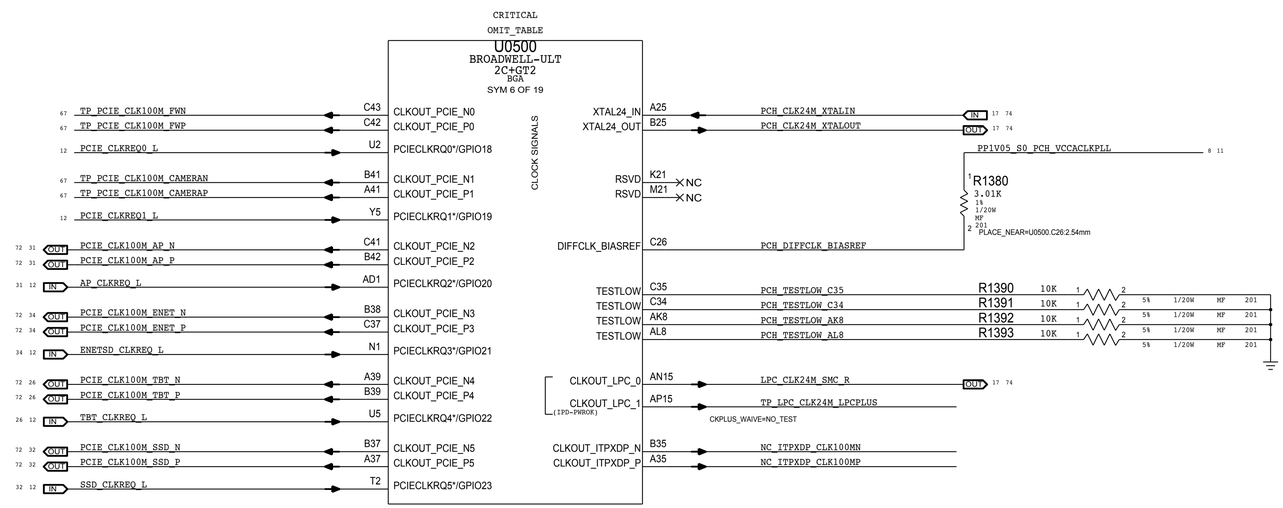
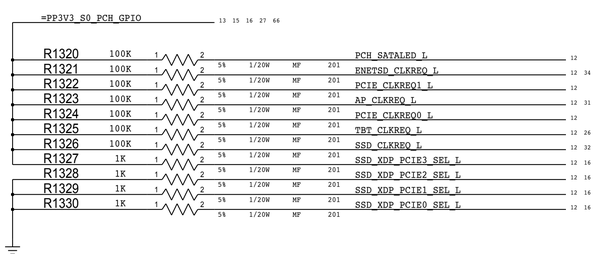


NOTE: Haswell ULT requires that CLQREQ_n be mapped to ROOT_PORT_n+1 to properly support CLKREQs for PCIE devices.





SYNC_MASTER=J117_TONY	SYNC_DATE=05/05/2014
PAGE TITLE	PCH Audio/JTAG/SATA/CLK
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
	REVISION 3.0.0
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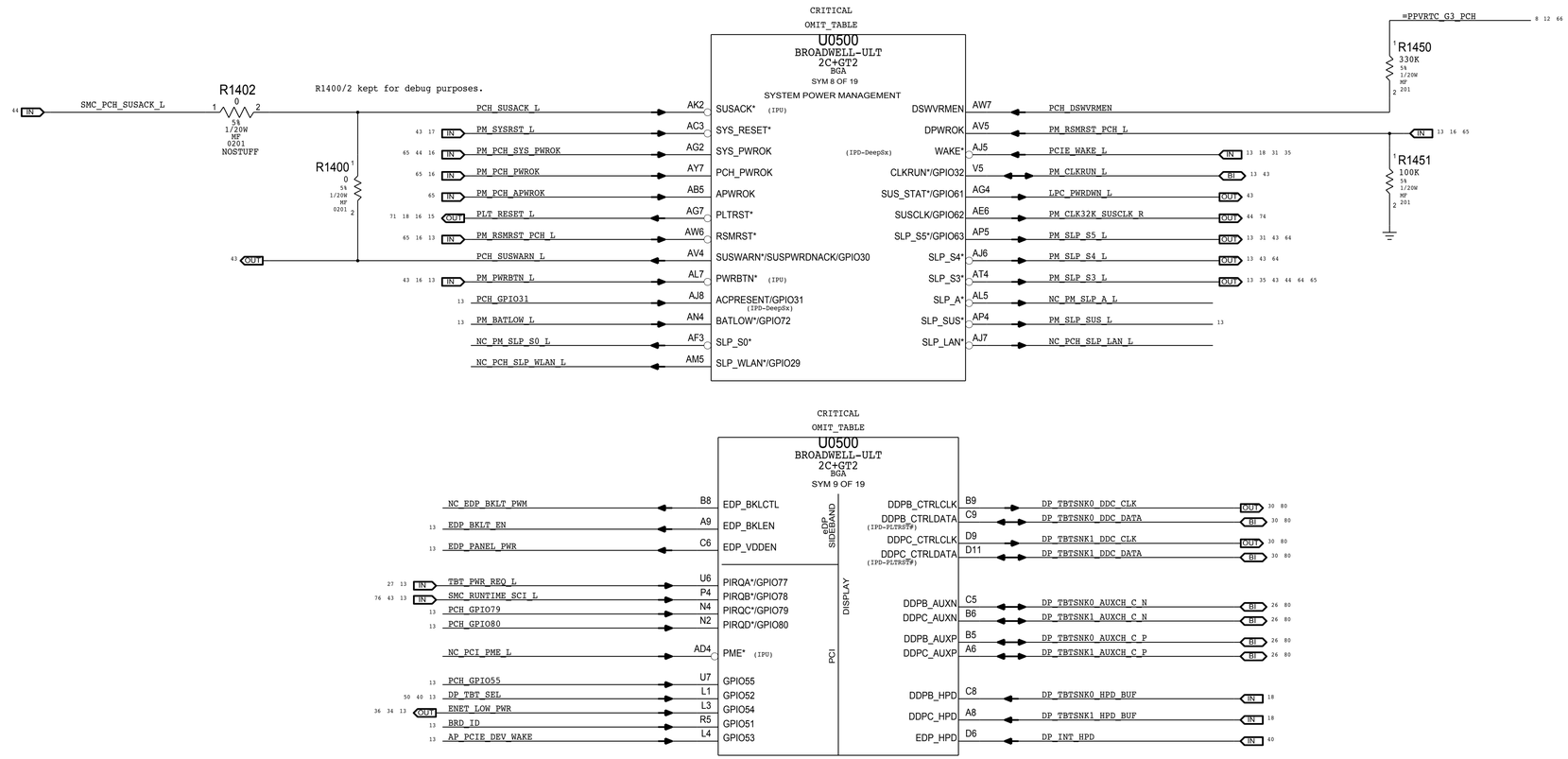

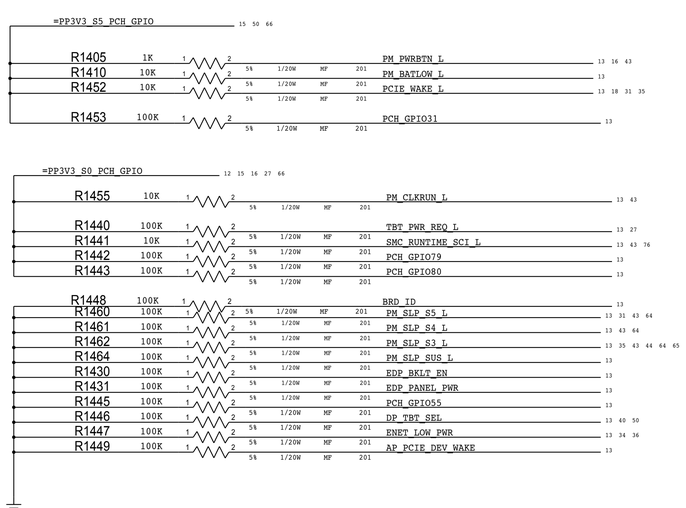

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

REVISION 3.0.0

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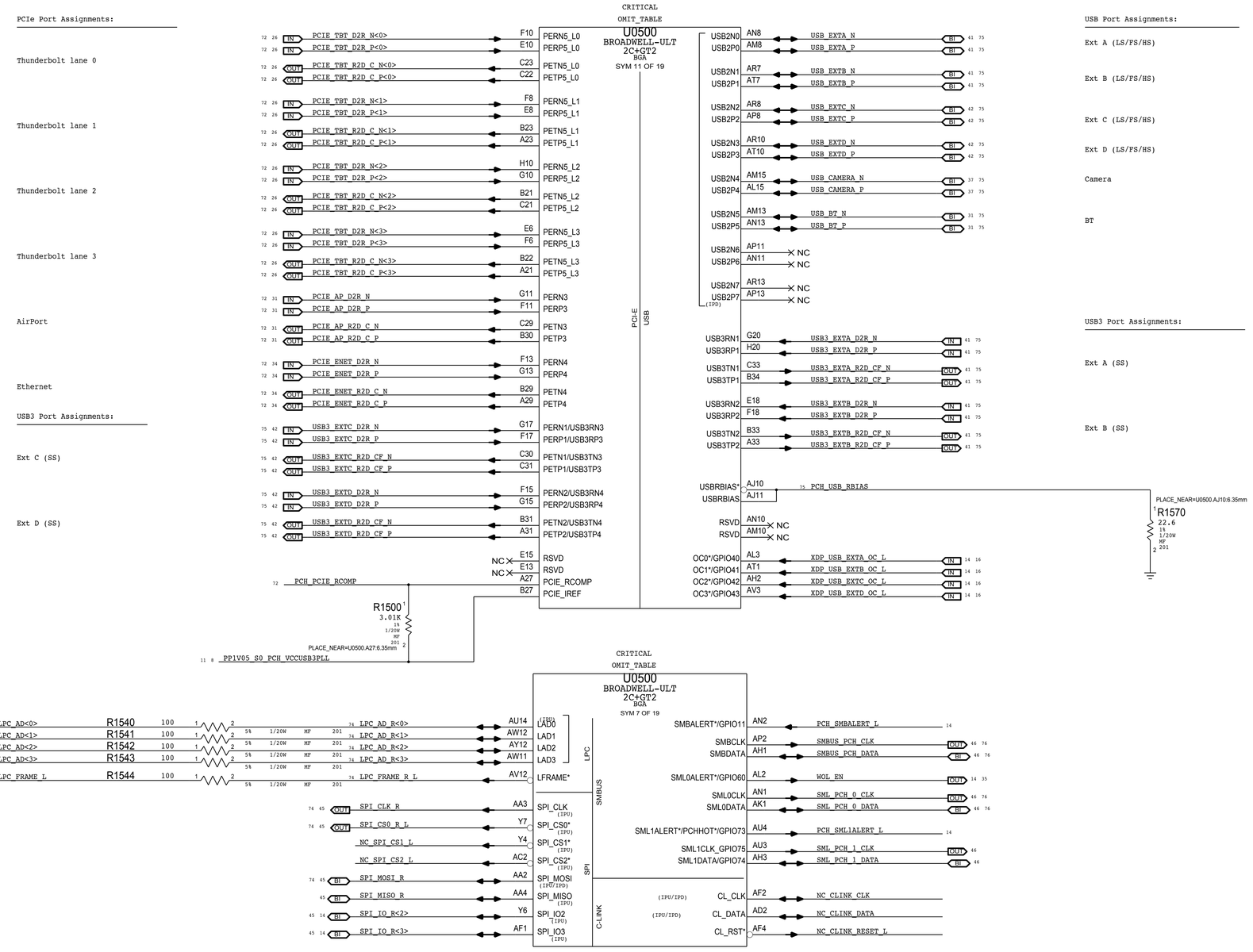

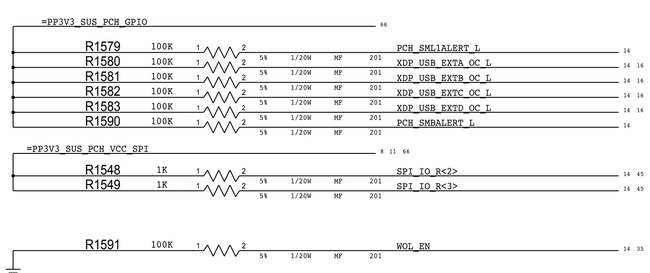

SYNC_MASTER=J117_ANDRES	SYNC_DATE=03/24/2014
PAGE TITLE	PCH PCIe/USB/LPC/SPI/SMBus
Apple Inc.	DRAWING NUMBER 051-00081 — SIZE D
	REVISION 3.0.0
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GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

Required JTAG pullups are on the XDP connector page.

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 10 OF 19

Signal	Pin	Net
MLB_RAMCFG4	P1	BMBUSY*/GPIO76
MLB_RAMCFG0	AU2	GPIO8
HDMITBTMUX_SEL_TBT	AM7	LAN_PHY_PWR_CTRL/GPIO12
NC_MEM_VDD_SEL_1V5_L (NO_TEST=1)	AD6	GPIO15 (IPD-RSMRST#)
XDP_LPCPLUS_GPIO	Y1	GPIO16
XDP_PCH_GPIO17	T3	GPIO17
ENET_SD_RESET_L	AD5	GPIO24
SMC_WAKE_SCI_L	AN5	GPIO27 (IPD-DeepSx)
TPAD_SPI_INT_L	AD7	GPIO28
ENET_MEDIA_SENSE	AN3	GPIO26
SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
HDD_PWR_EN	AL4	GPIO58
XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
SD_PWR_EN	AK4	GPIO44
TBT_PWR_EN	AB6	GPIO47
XDP_JTAG_ISP_TCK	U4	GPIO48
XDP_JTAG_ISP_TDI	Y3	GPIO49
JTAG_TBT_TMS_PCH	P3	GPIO50
PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
TPAD_SPI_IF_EN	AT3	GPIO13
MLB_RAMCFG3	AH4	GPIO14
SPIROM_USE_MLB	AM4	GPIO25
SSD_RESET_L	AG5	GPIO45
SSD_SR_EN_L	AG3	GPIO46
MLB_RAMCFG1	AM3	GPIO9
MLB_RAMCFG2	AM2	GPIO10
PCH_GPIO33	P2	DEVSLP0/GPIO33
AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
PCH_GPIO38	L2	DEVSLP1/GPIO38
PCH_GPIO39	N5	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD-PLTRST#)

Signal	Pin	Net
THERMTRIP*	D60	PM_THRMTRIP_L
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT_L
SERIRQ	T4	LPC_SERIRQ
PCH_OPI_COMP	AW15	PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC
GSPI0_CS*/GPIO83	R6	MEM_GOOD_LED
GSPI0_CLK/GPIO84	L6	PCH_CAM_RESET_L
GSPI0_MISO/GPIO85 (IPD)	N6	PCH_CAM_EXT_BOOT
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	AUD_SPI_MOSI
GSPI1_CS*/GPIO87	R7	PCH_GSPI1_CS_L
GSPI1_CLK/GPIO88	L5	SDCONN_OC_L
GSPI1_MISO/GPIO89 (IPD)	N7	PCH_GSPI1_MISO
GSPI_MOSI/GPIO90	K2	PCH_GSPI1_MOSI
UART0_RXD/GPIO91	J1	AP_S0IX_WAKE_L
UART0_TXD/GPIO92	K3	HDMITBTMUX_FLAG_L
UART0_RTS*/GPIO93	J2	PCH_BT_UART_RTS_L
UART0_CTS*/GPIO94	G1	PCH_BT_UART_CTS_L
UART1_RXD/GPIO0	K4	PCH_UART1_RXD
UART1_TXD/GPIO1	G2	PCH_UART1_TXD
UART1_RST*/GPIO2	J3	JTAG_ISP_TDO
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L
I2C0_SDA/GPIO4	F2	PCH_GPIO4
I2C0_SCL/GPIO5	F3	AP_RESET_L
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L
SDIO_CMD/GPIO65	F4	BT_PWR_RST_L
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	E4	PCH_GPIO67
SDIO_D2/GPIO68	C3	LCD_IRQ_L
SDIO_D3/GPIO69	E2	LCD_PSR_EN

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

Pull-up on TBT page

Requires connection to SMC via 1K series R

RAM Configuration Straps

For chip-down RAM systems

Resistor	Value	Signal	Strap
R1688	100K	MLB_RAMCFG0	RAMCFG4:H
R1680	100K	MLB_RAMCFG1	RAMCFG3:H
R1681	100K	MLB_RAMCFG2	RAMCFG2:H
R1682	100K	MLB_RAMCFG3	RAMCFG1:H
R1683	100K	MLB_RAMCFG4	RAMCFG0:H
R1689	10K	MLB_RAMCFG0	RAMCFG4:L
R1684	10K	MLB_RAMCFG1	RAMCFG3:L
R1685	10K	MLB_RAMCFG2	RAMCFG2:L
R1686	10K	MLB_RAMCFG3	RAMCFG1:L
R1687	10K	MLB_RAMCFG4	RAMCFG0:L

Resistor	Value	Signal	Page
R1628	100K	PCH_GPIO38	15
R1624	100K	JTAG_TBT_TMS_PCH	15 18
R1634	100K	JTAG_ISP_TDO	15 18
R1609	100K	TBT_CIO_PLUG_EVENT_L	15 26
R1611	100K	XDP_LPCPLUS_GPIO	15 16
R1618	100K	HDD_PWR_EN	15 63
R1621	100K	TBT_PWR_EN	15 26
R1625	100K	PCH_HSIO_PWR_EN	15
R1630	100K	PCH_GPIO33	15
R1632	100K	PCH_GPIO39	15
R1633	10K	LPC_SERIRQ	15 43
R1635	100K	BT_PWR_RST_L	15
R1637	100K	LCD_IRQ_L	15
R1617	100K	SSD_PWR_EN	15 63
R1629	100K	SSD_SR_EN_L	15 32
R1615	100K	TPAD_SPI_INT_L	15
R1619	100K	XDP_SDCONN_STATE_CHANGE_L	15 16
R1620	100K	SD_PWR_EN	15
R1614	100K	SMC_WAKE_SCI_L	15 43 76
R1613	100K	SPIROM_USE_MLB	15 45 74
R1616	100K	PCH_GPIO67	15
R1612	100K	XDP_PCH_GPIO17	15 16
R1622	100K	XDP_JTAG_ISP_TCK	15 16 18
R1623	100K	XDP_JTAG_ISP_TDI	15 16 18
R1626	100K	TPAD_SPI_IF_EN	15
R1631	100K	AP_S0IX_WAKE_SEL	15
R1636	100K	ENET_MEDIA_SENSE	15 34 75
R1638	100K	LCD_PSR_EN	15

TBTLC for CR, S0 for RR

Resistor	Value	Signal	Page
R1658	100K	AP_S0IX_WAKE_L	15
R1659	100K	HDMITBTMUX_FLAG_L	15
R1666	100K	PCH_I2C1_SDA	15
R1667	100K	PCH_I2C1_SCL	15
R1661	47K	PCH_UART1_TXD	15
R1654	47K	PCH_GSPI1_CS_L	15
R1653	47K	PCH_GSPI1_MOSI	15
R1664	47K	PCH_GPIO4	15
R1651	47K	SDCONN_OC_L	36 15
R1657	100K	AUD_SPI_MOSI	15
R1650	100K	MEM_GOOD_LED	15 3
R1668	100K	PCH_CAM_RESET_L NOSTUFF	38 15
R1669	100K	PCH_CAM_EXT_BOOT NOSTUFF	38 15
R1670	47K	PCH_BT_UART_RTS_L	15
R1671	47K	PCH_BT_UART_CTS_L	15
R1660	47K	PCH_UART1_RXD	15
R1663	47K	PCH_UART1_CTS_L	15
R1652	47K	PCH_GSPI1_MISO	15

Resistor	Value	Net	Page
R1600	1K	=PP1V05_S0_CPU_VCCST	66 57 17 16 8 6
R1601	49.9	PLACE_NEAR=U0500.AW15:12.7mm	
R1602	100K	PLT_RESET_L	13 15 16 18 71
R1603	100K		36
R1604	1K		26
R1605	1K	=PP3V3_S0_PCH_GPIO	66 27 16 15 13 12
R1606	100K	PLT_RESET_L	71 18 16 15 13

=PP3V3_S5_PCH_GPIO 13 50 66
=PP3V3_S4_PCH_GPIO 18 41 42 66
=PP3V3_S0_PCH_GPIO 12 13 15 16 27 66

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014
PAGE TITLE
PCH GPIO/MISC/LPIO
Apple Inc.
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Extra BPM Testpoints

XDP_BPM_L<2>	TP1802	TP-P6
XDP_BPM_L<3>	TP1803	TP-P6
XDP_BPM_L<4>	TP1804	TP-P6
XDP_BPM_L<5>	TP1805	TP-P6
XDP_BPM_L<6>	TP1806	TP-P6
XDP_BPM_L<7>	TP1807	TP-P6

CPU Micro2-XDP

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

=PP1V05_S0_XDP — R1832 150 5% 1/16W MF-LF 402

OMIT XW1800 SHORT 402

OMIT XW1801 SHORT 402

PPVCCIO_S0_CPU

Signal	Pin	Pin	Signal
XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	TTPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	TTPCLK#/HOOK5	NC
XDP_CPU_OBSAB	VCC_OBS_AB	VCC_OBS_CD	XDP_CPU_OBSCD
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
TP_XDP_TCK1	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CPU_VCCST_PWRGD	R1800	1K	PLACE_NEAR=U0500.C61:12.7mm
PM_PWRBTN_L	R1802	0	PLACE_NEAR=U5000.J3:12.7mm
PM_PCH_SYS_PWROK	R1804	220	5% 1/16W MF-LF 402

R1805 1K 5% 1/20W MF 201 — PLT_RESET_L — PLACE_NEAR=U0500.AG7:12.7mm

=PP1V05_S0_CPU_VCCST

XDP_CPU_TDO	R1810	51	PLACE_NEAR=J1800.51:28mm
XDP_CPU_TRST_L	R1811	51	PLACE_NEAR=U0500.E59:28mm
XDP_CPU_TCK	R1813	51	PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.48:28mm

R1831 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U0500.AA63:50mm

C1800 0.1UF 10% 6.3V CERM-X5R 0201

C1801 0.1UF 10% 6.3V CERM-X5R 0201

C1806 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.47:28mm

XDP_CPU_PRESENT_L

1.05V S5 LDO

Power to the JTAG debug lines

=PP3V3_S5_PWRCTL

C1830 0.1UF 10% 16V X7R-CERM 0402

R1833 150 5% 1/16W MF-LF 402

PM_EN_REG_P1V05_S5

C1832 0.1UF 10% 6.3V CERM-X5R 0201

U1830
TPS720105
SON
CRITICAL
XDP

BIAS, IN, EN, OUT, NC, GND, THRM PAD

PP1V05_S5 — C1831 2.2UF 10% 6.3V X5R 402

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500

PP1V05_S5

R1890	51 1% 1/20W MF 201	XDP_PCH_TDO
R1891	51 1% 1/20W MF 201	XDP_PCH_TDI
R1892	51 1% 1/20W MF 201	XDP_PCH_TMS
R1899	1K 1% 1/20W MF 201	PCH_JTAGX

NOSTUFF

XDP_PCH_TCK	R1896	51	PLACE_NEAR=U0500.AE62:28mm
XDP_PCH_TRST_L	R1897	51	PLACE_NEAR=U0500.AU62:28mm

NOSTUFF

R1881 1K 5% 1/20W MF 201 — XDP_PM_PCH_PWROK — PM_PCH_PWROK

R1882 0 5% 1/20W MF 0201 NOSTUFF — XDP_PCH_TRST_L_R — XDP_PCH_TRST_L

PCH_JTAGX — R1835 0 5% 1/20W MF — PCH_JTAGX_R — TP1888 — PLACE_NEAR=J1800.58:28mm

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals	Non-XDP Signals
XDP_USB_EXTA_OC_L	USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	USB_EXTD_OC_L
XDP_MLB_RAMCFG0	MLB_RAMCFG0
XDP_MLB_RAMCFG1	MLB_RAMCFG1
XDP_MLB_RAMCFG2	MLB_RAMCFG2
XDP_MLB_RAMCFG3	MLB_RAMCFG3
XDP_MLB_RAMCFG4	MLB_RAMCFG4
XDP_SDCONN_STATE_CHANGE_L	SDCONN_STATE_CHANGE_L

MAKE_BASE=TRUE

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM1

OMIT XW1850 SHORT 402

Signal	Pin	Pin	Signal
	OBSFN_A0	OBSFN_C0	XDP_MLB_RAMCFG0
	OBSFN_A1	OBSFN_C1	XDP_JTAG_ISP_TCK
XDP_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	SSD_XDP_PCIE3_SEL_L
XDP_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	SSD_XDP_PCIE2_SEL_L
XDP_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	SSD_XDP_PCIE1_SEL_L
XDP_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	SSD_XDP_PCIE0_SEL_L
	OBSFN_B0	OBSFN_D0	
	OBSFN_B1	OBSFN_D1	
XDP_SDCONN_STATE_CHANGE_L	OBSDATA_B0	OBSDATA_D0	XDP_LPCPLUS_GPIO
XDP_MLB_RAMCFG1	OBSDATA_B1	OBSDATA_D1	XDP_PCH_GPIO17
XDP_MLB_RAMCFG2	OBSDATA_B2	OBSDATA_D2	XDP_MLB_RAMCFG4
XDP_MLB_RAMCFG3	OBSDATA_B3	OBSDATA_D3	XDP_JTAG_ISP_TDI
PM_RSMRST_PCH_L	HOOK0	HOOK4	=PP1V05_S0_XDP
XDP_CPU_PWRBTN_L	HOOK1	HOOK5	
XDP_PCH_OBSAB	VCC_OBS_AB	VCC_OBS_CD	=PP3V3_S0_PCH_GPIO
	HOOK2	HOOK6	XDP_PM_PCH_PWROK
	HOOK3	HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_PCH_TRST_L_R
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS

R1883 1K 5% 1/20W MF 201 — XDP_PM_RSMRST_PCH_L

C1850 0.1UF 10% 6.3V CERM-X5R 0201

C1851 0.1UF 10% 6.3V CERM-X5R 0201

C1852 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1850.47:28mm

MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=J117_ANDRES — SYNC_DATE=03/24/2014

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: 051-00081 — SIZE: D

REVISION: 3.0.0

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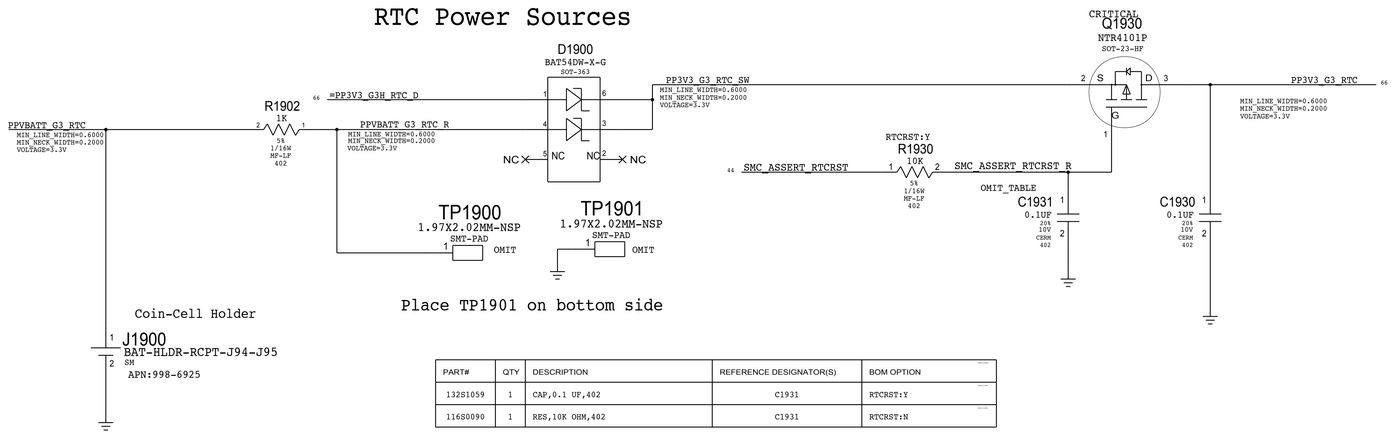
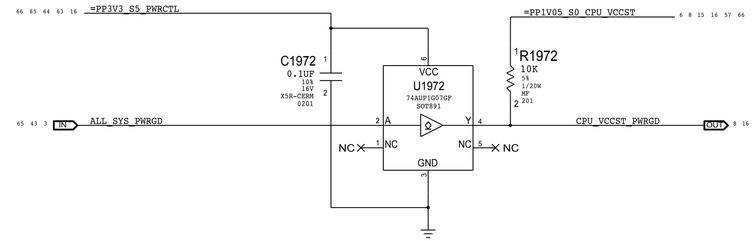
RTC Power Sources

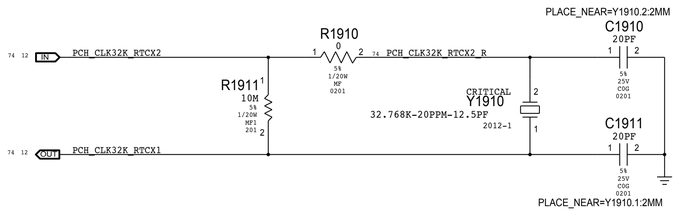


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K OHM,402	C1931	RTCRST:N

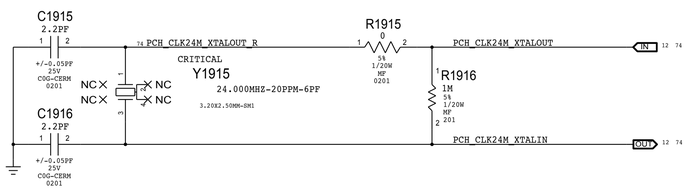
ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter



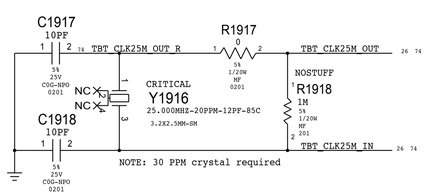
PCH RTC Crystal



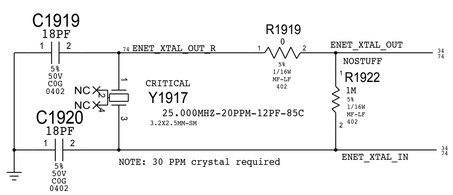
PCH 24MHz Crystal



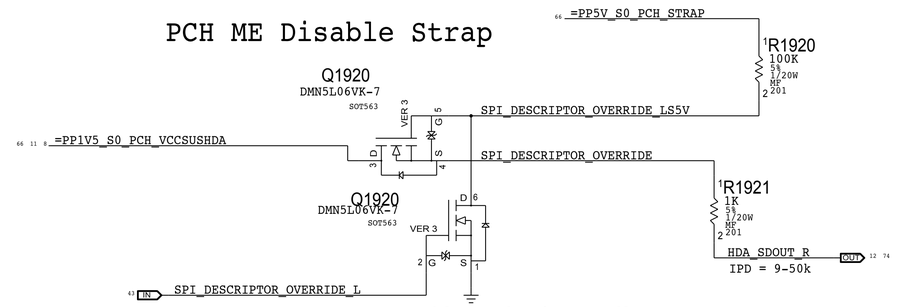
TBT 25MHz Crystal



Ethernet 25MHz Crystal

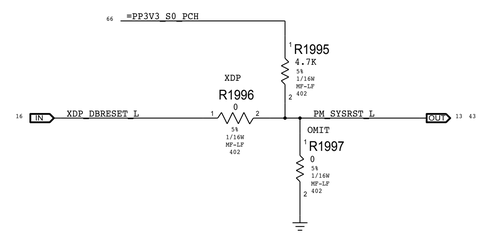


PCH ME Disable Strap

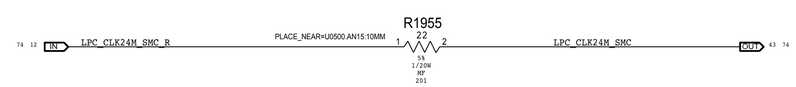


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH Reset Button



Clock series termination



SYNC_MASTER=J70_NICK SYNC_DATE=02/25/2014

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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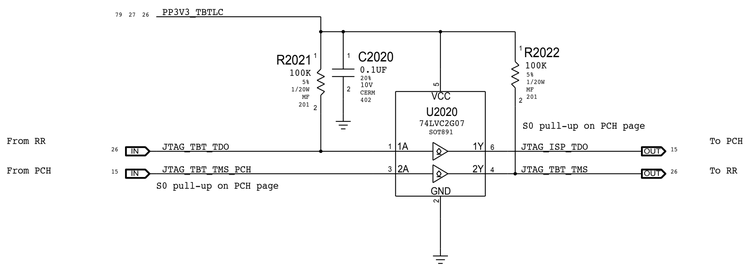
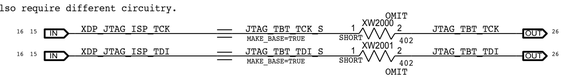
Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

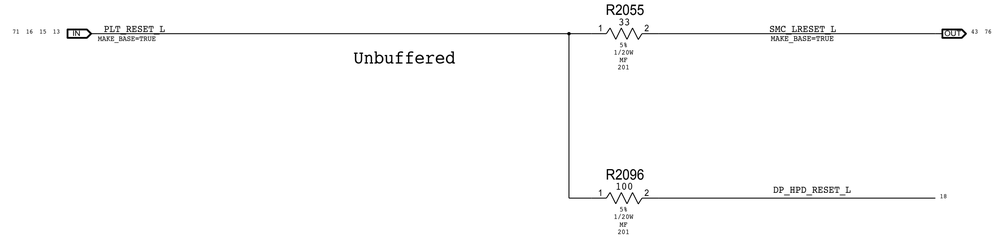


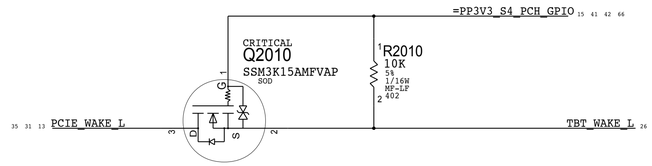
NOTE: Solution shown is for WPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.



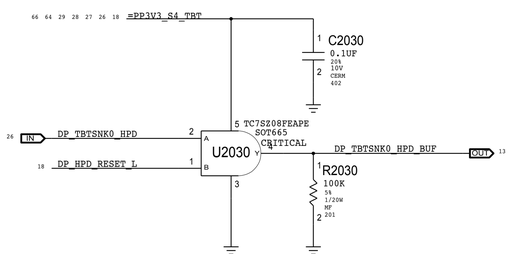
Platform Reset Connections

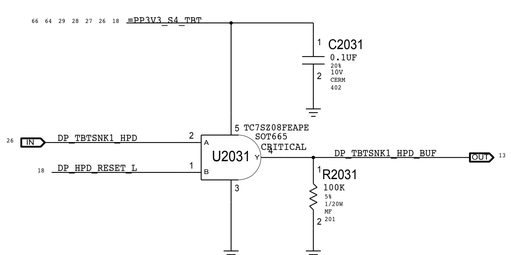




Falcon Ridge HPD Isolation

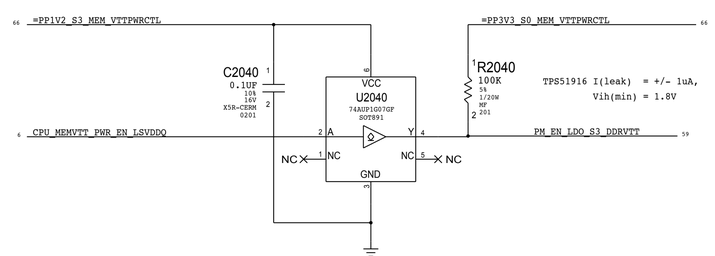
NOTE: PLT_RESET_L used as the other input to the AND gate so that HPD is only driven high to the PCH in S0.





Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



SYNC_MASTER=J70_NICK	SYNC_DATE=11/20/2013
PAGE TITLE: Project Chipset Support	
Apple Inc.	DRAWING NUMBER: 051-00081 — SIZE: D
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Memory Bit/Byte Swizzle

		MAKE_BASE		
21	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<0>	? ?0
21	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<1>	? ?0
21	=MEM_A_DQ<2>	TRUE	MEM_A_DQ<2>	? ?0
21	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<3>	? ?0
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21	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<7>	? ?0
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23	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<3>	? ?0
24	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<4>	? ?0
24	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<4>	? ?0
24	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<5>	? ?0
24	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<5>	? ?0
24	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	? ?0
24	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	? ?0
24	=MEM_B_DQS_P<7>	TRUE	MEM_B_DQS_P<7>	? ?0
24	=MEM_B_DQS_N<7>	TRUE	MEM_B_DQS_N<7>	? ?0

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DDR3 Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

REVISION 3.0.0

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PAGE 21 OF 123

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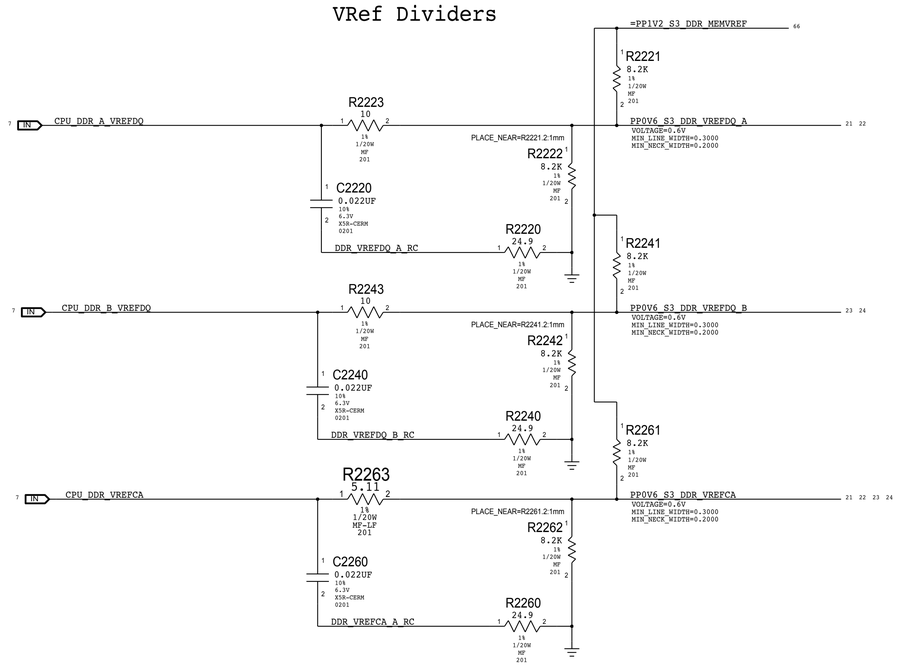
VRef Dividers



SYNC_MASTER=J117_ANDRES SYNC_DATE=02/27/2014

PAGE TITLE

DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-00081

SIZE D

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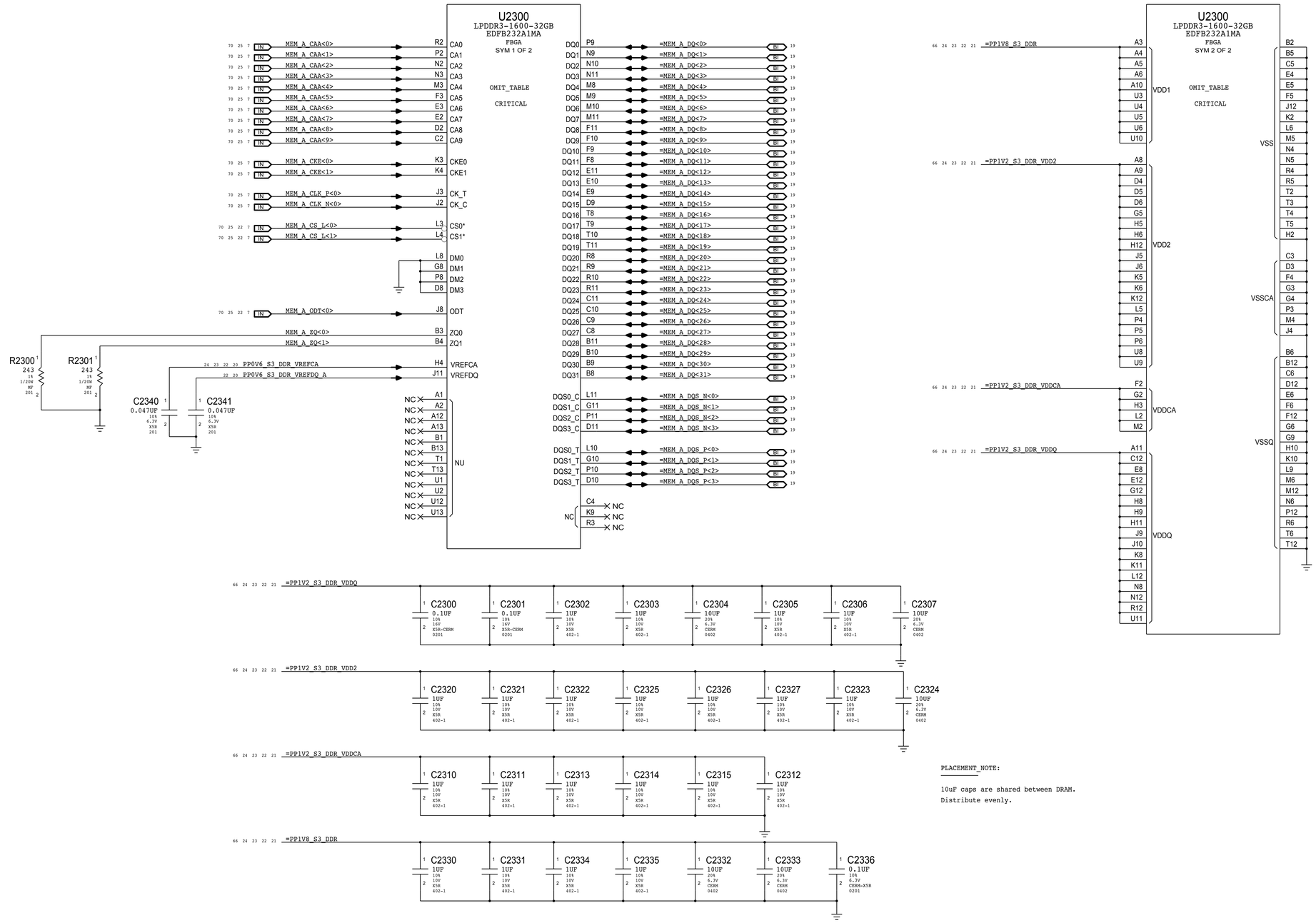
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER 051-00081

SIZE D

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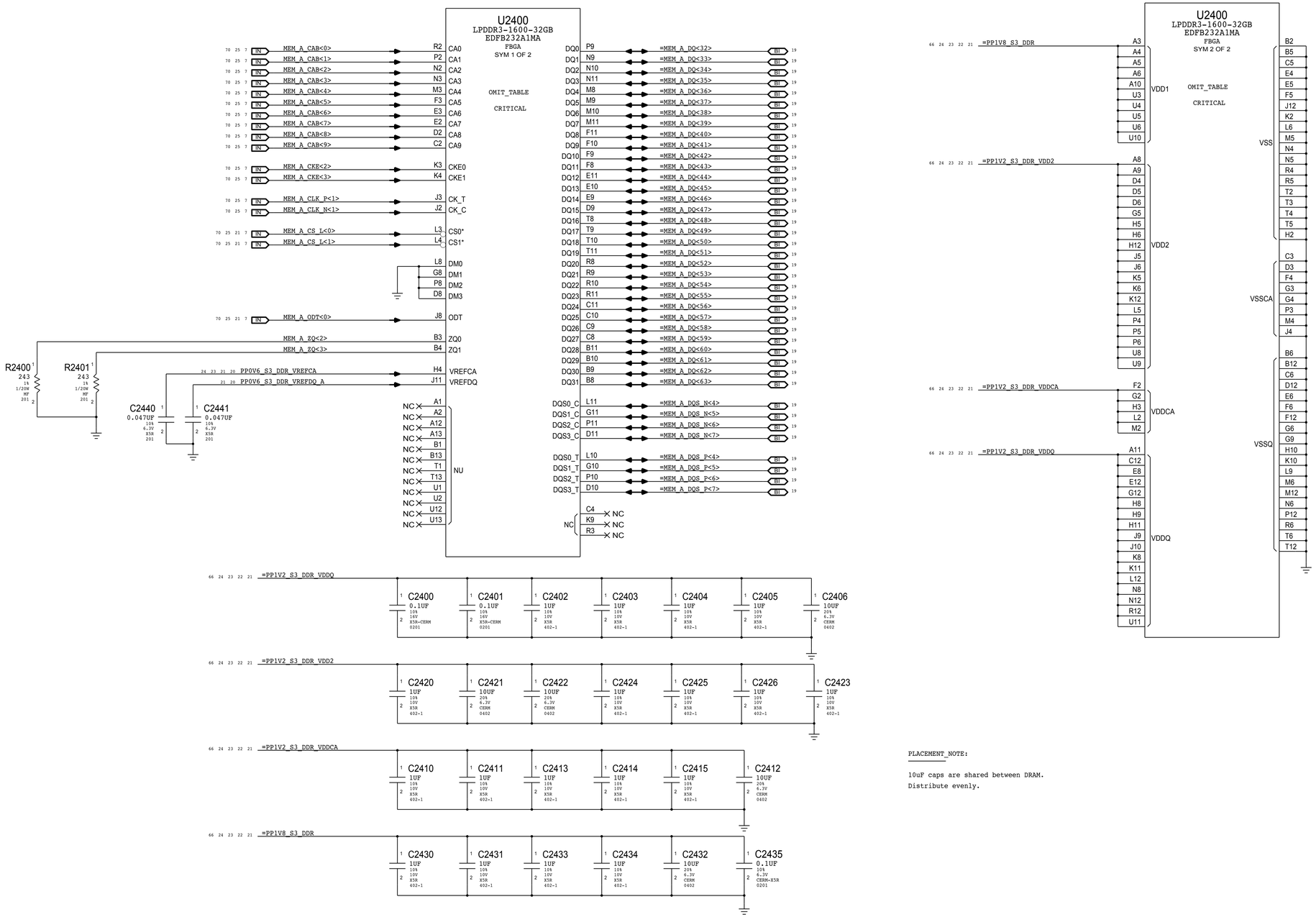
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB	SYNC_DATE=09/03/2013
PAGE TITLE: LPDDR3 DRAM Channel A (32-63)	
Apple Inc.	DRAWING NUMBER: 051-00081 — SIZE: D
	REVISION: 3.0.0
	BRANCH
	PAGE: 24 OF 123
	SHEET: 22 OF 81

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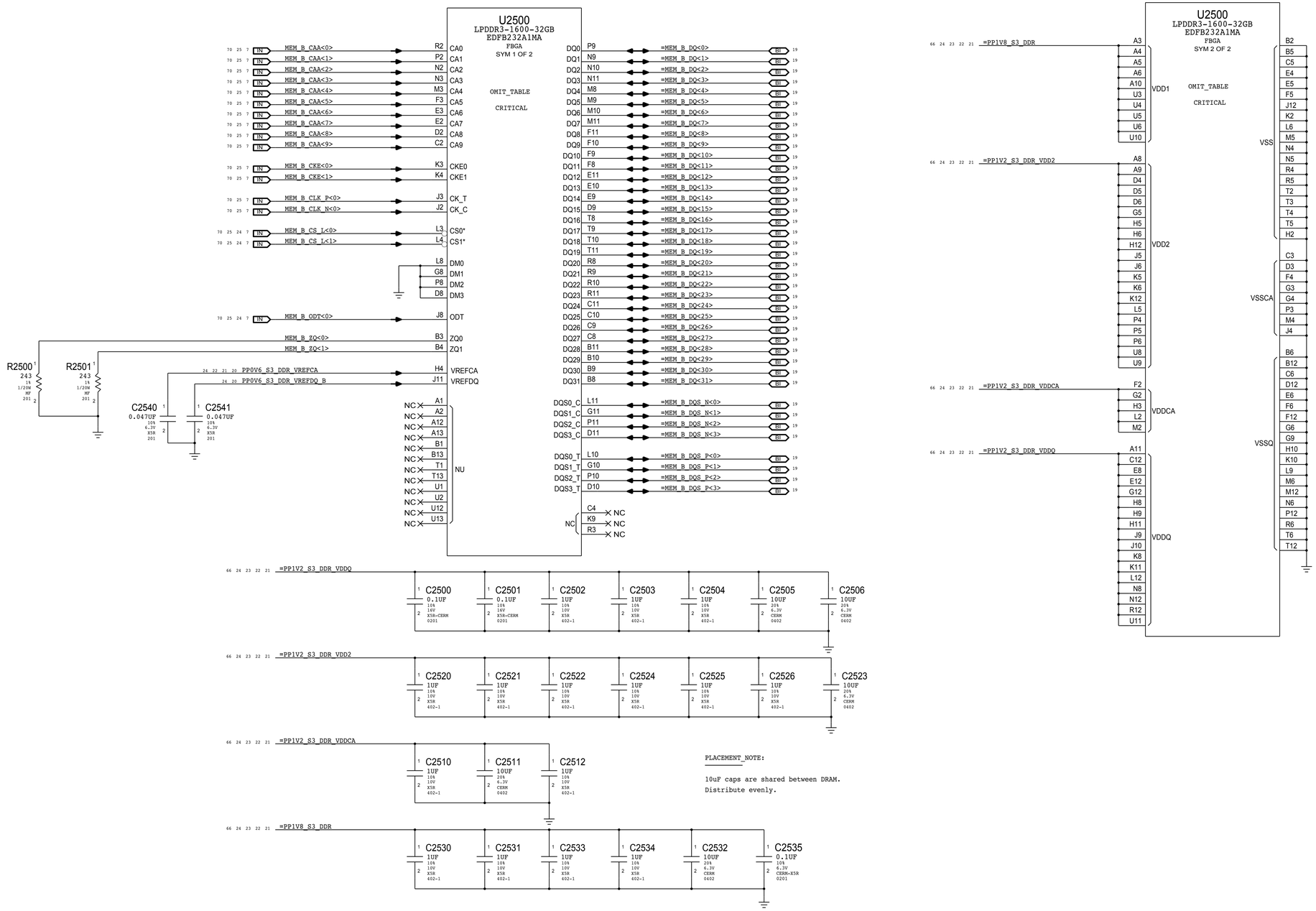
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel B (0-31)

Apple Inc.

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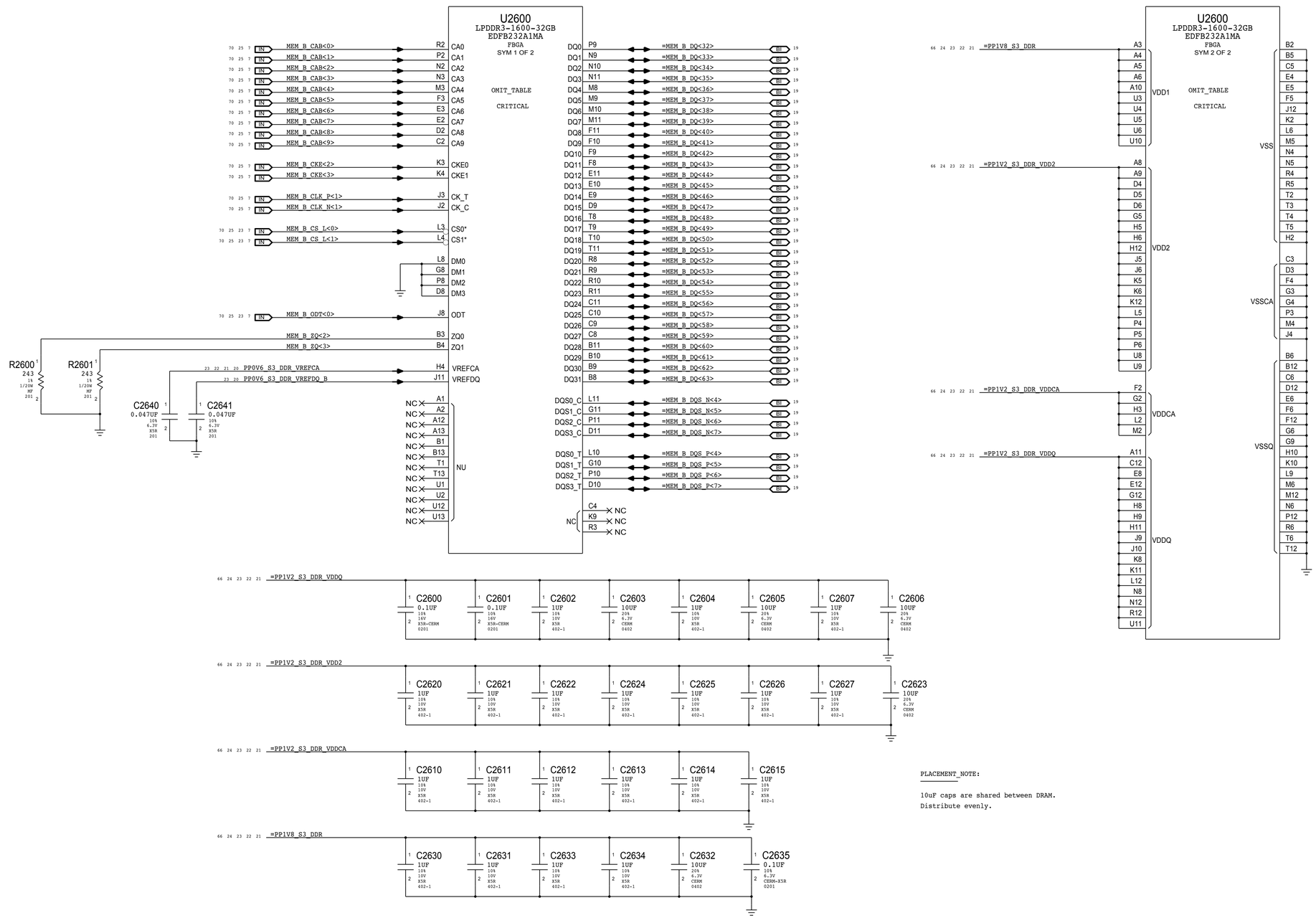
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel B (32-63)

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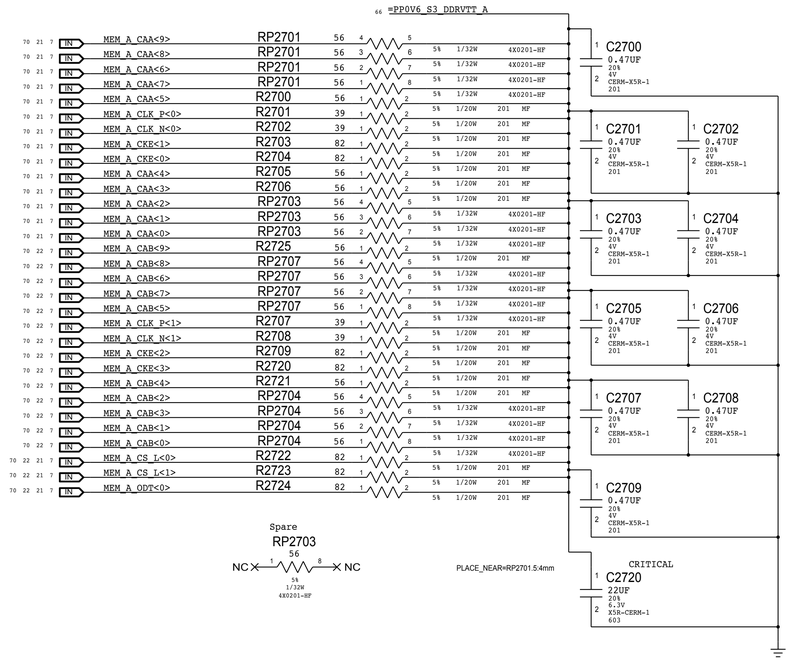
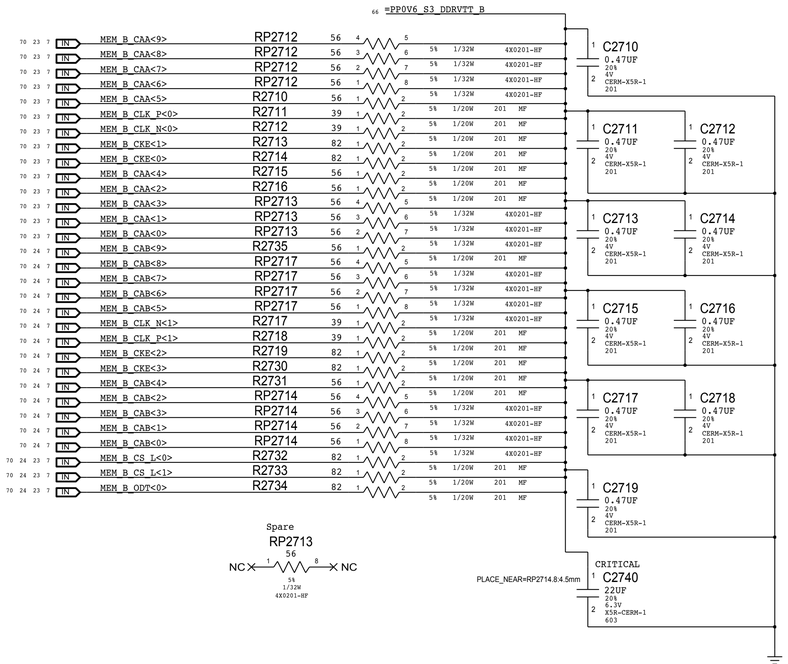
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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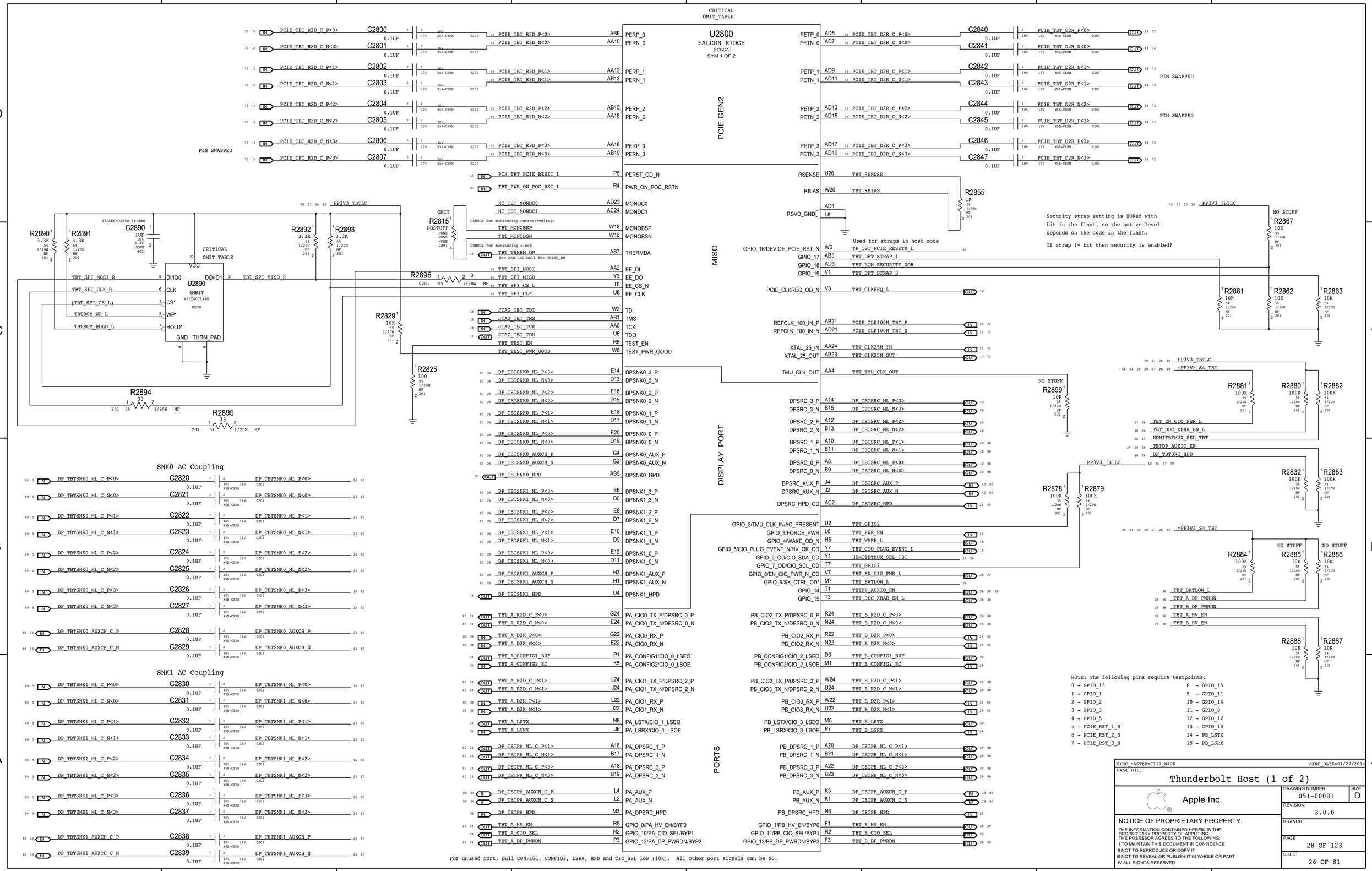
U2800
FALCON RIDGE
PCBGA
SYM 1 OF 2
CRITICAL
OMIT_TABLE
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PIN SWAPPED
SNK0 AC Coupling
SNK1 AC Coupling
U2890
4MBIT
W25X40CLXIG
USON
Security strap setting is XORed with
bit in the flash, so the active-level
depends on the code in the flash.
If strap != bit then security is enabled?
Used for straps in host mode
NO STUFF
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J117_NICK
SYNC_DATE=01/27/2014
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
051-00081
SIZE
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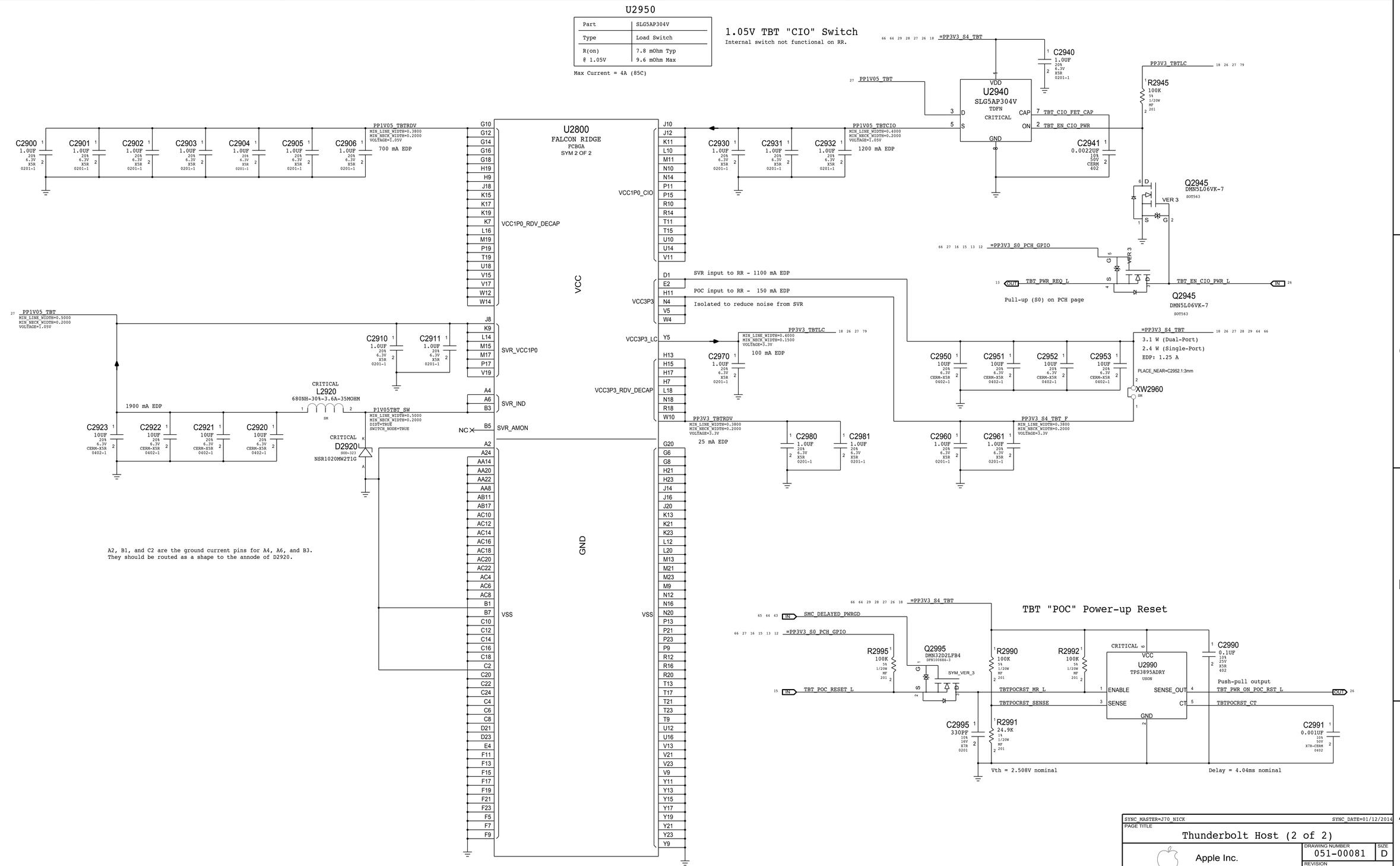

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=J70_NICK SYNC_DATE=01/12/2014

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0398	128S0220		ALL	3.3V INPUT CAP

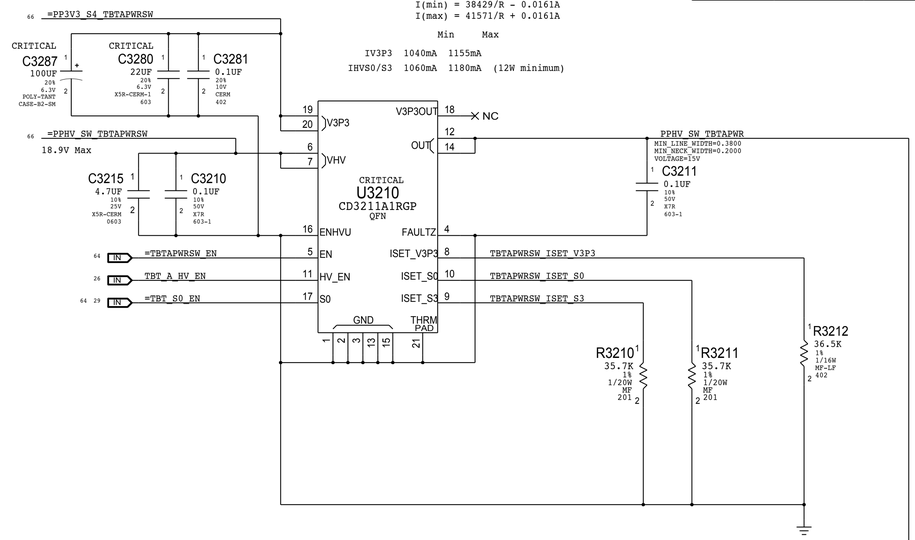
3.3V/HV Power MUX

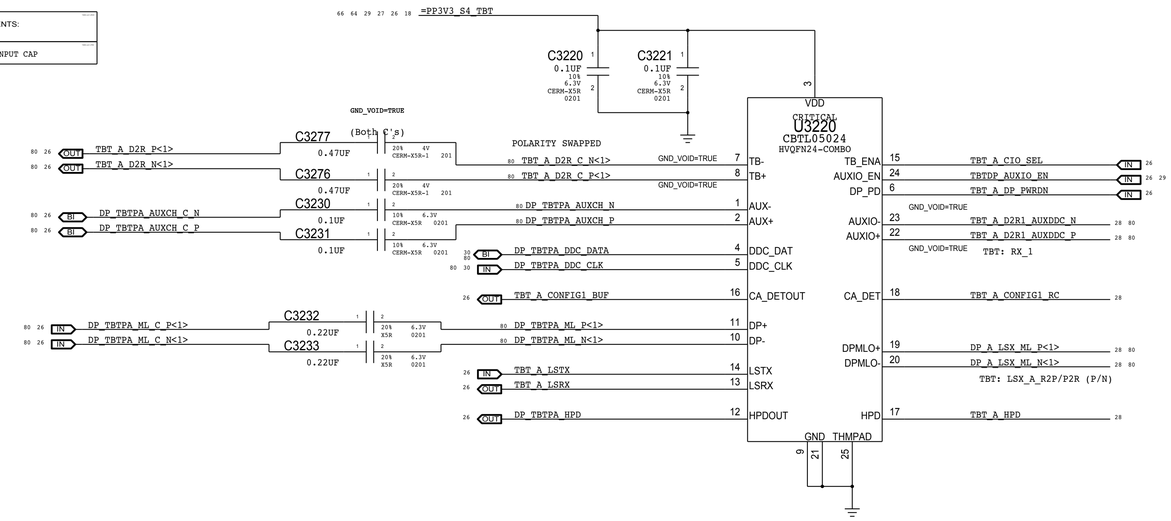
V3P3 must be S4 to support wake from Thunderbolt devices.

For 12V systems:

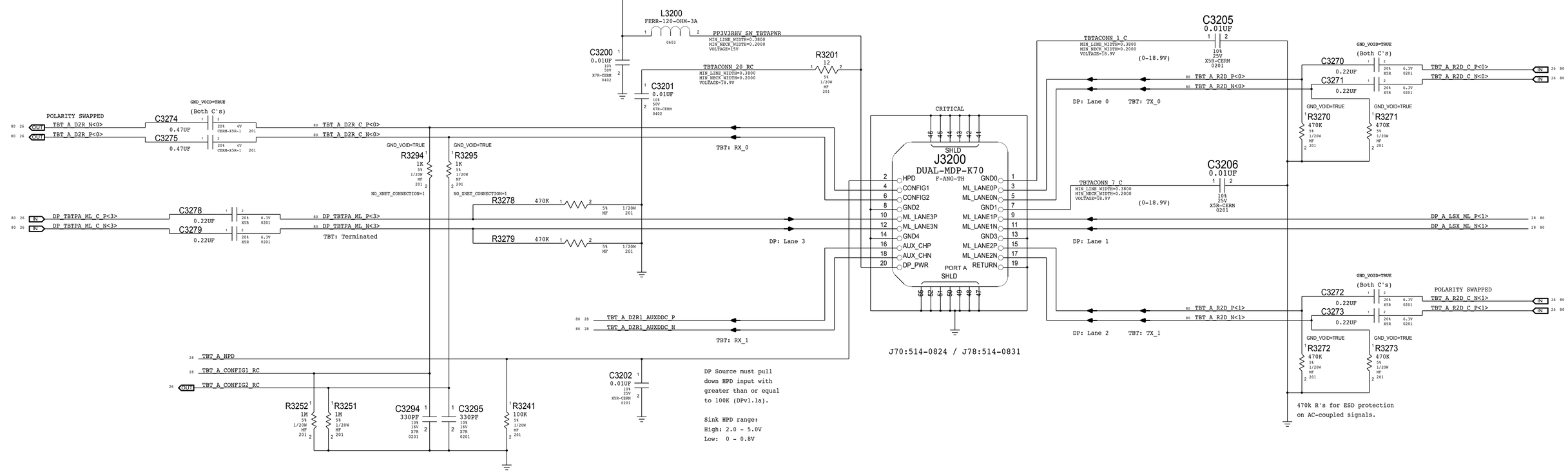
I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max
IV3P3	1040mA	1155mA
IHVS0/S3	1060mA	1180mA (12W minimum)





Thunderbolt Connector A



SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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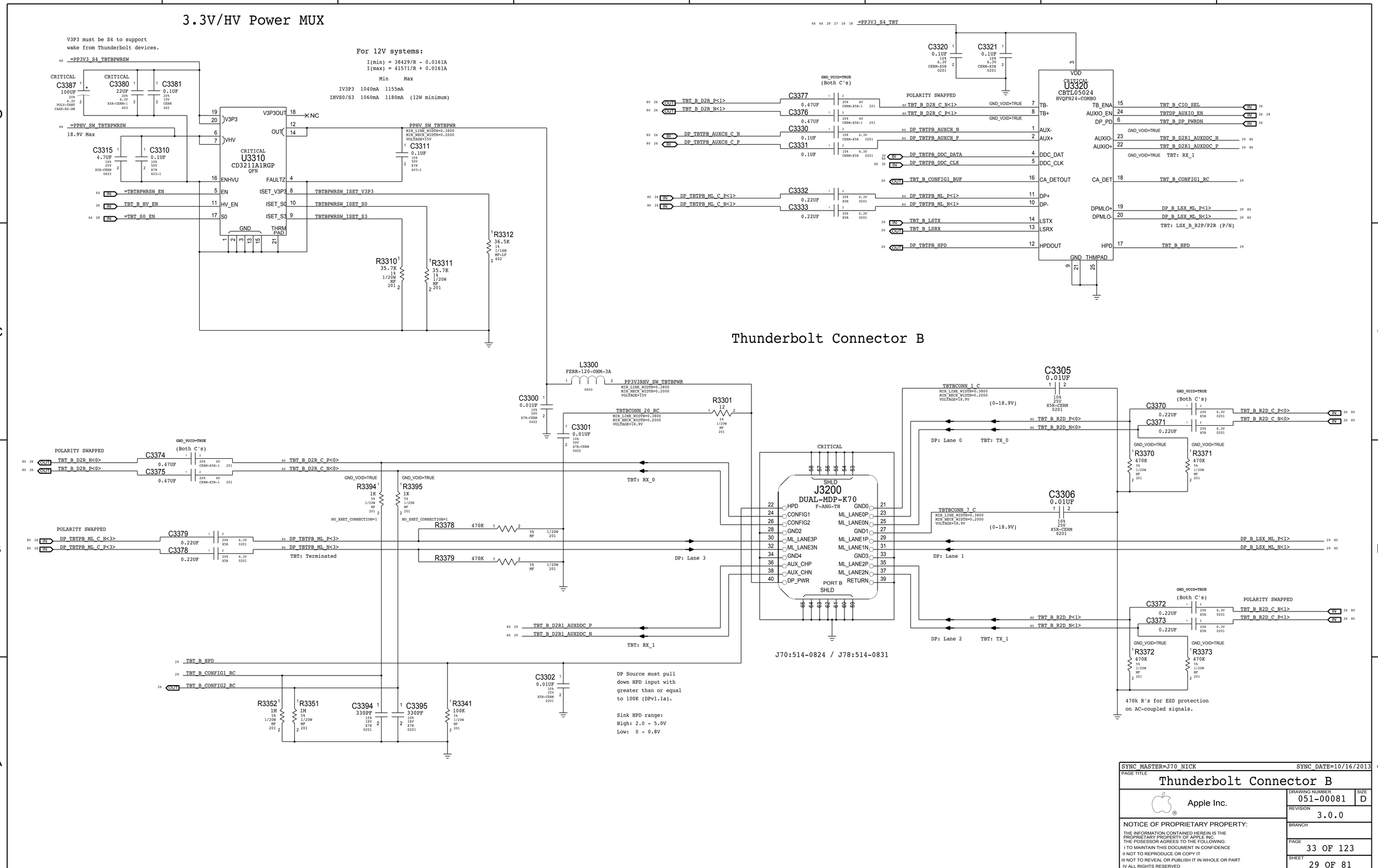
3.3V/HV Power MUX
V3P3 must be S4 to support wake from Thunderbolt devices.
For 12V systems:
I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A
Min Max
IV3P3 1040mA 1155mA
IHVS0/S3 1060mA 1180mA (12W minimum)
=PP3V3_S4_TBTBPWRSW
=PPHV_SW_TBTBPWRSW
18.9V Max
CRITICAL
C3387 100UF
C3380 22UF
C3381 0.1UF
C3315 4.7UF
C3310 0.1UF
U3310
CD3211A1RGP
QFN
V3P3
VHV
V3P3OUT
OUT
ENHVU
EN
HV_EN
S0
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
THRM PAD
GND
NC
PPHV_SW_TBTBPWR
C3311 0.1UF
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
R3310 35.7K
R3311 35.7K
R3312 36.5K
=PP3V3_S4_TBT
C3320 0.1UF
C3321 0.1UF
VDD
U3320
CBTL05024
HVQFN24-COMBO
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND_THMPAD
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
TBT_B_CIO_SEL
TBTDP_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_B_R2P/P2R (P/N)
TBT_B_HPD
Thunderbolt Connector B
L3300
FERR-120-OHM-3A
PP3V3RHV_SW_TBTBPWR
C3300 0.01UF
C3301 0.01UF
TBTBCONN_20_RC
R3301 12
C3305 0.01UF
TBTBCONN_1_C
(0-18.9V)
C3306 0.01UF
TBTBCONN_7_C
C3370 0.22UF
C3371 0.22UF
C3372 0.22UF
C3373 0.22UF
R3370 470K
R3371 470K
R3372 470K
R3373 470K
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
DP: Lane 0
TBT: TX_0
TBT: RX_0
C3374 0.47UF
C3375 0.47UF
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
R3394 1K
R3395 1K
NO_XNET_CONNECTION=1
C3379 0.22UF
C3378 0.22UF
DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_P<3>
DP_TBTPB_ML_N<3>
TBT: Terminated
R3378 470K
R3379 470K
DP: Lane 3
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
DP: Lane 1
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
DP: Lane 2
TBT: TX_1
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT: RX_1
CRITICAL
J3200
DUAL-MDP-K70
F-ANG-TH
SHLD
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT B SHLD
J70:514-0824 / J78:514-0831
C3352 1M
R3351 1M
C3394 330PF
C3395 330PF
R3341 100K
C3302 0.01UF
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
470k R's for ESD protection on AC-coupled signals.
SYNC_MASTER=J70_NICK
SYNC_DATE=10/16/2013
PAGE TITLE
Thunderbolt Connector B
Apple Inc.
DRAWING NUMBER 051-00081
SIZE D
REVISION 3.0.0
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SHEET 29 OF 81
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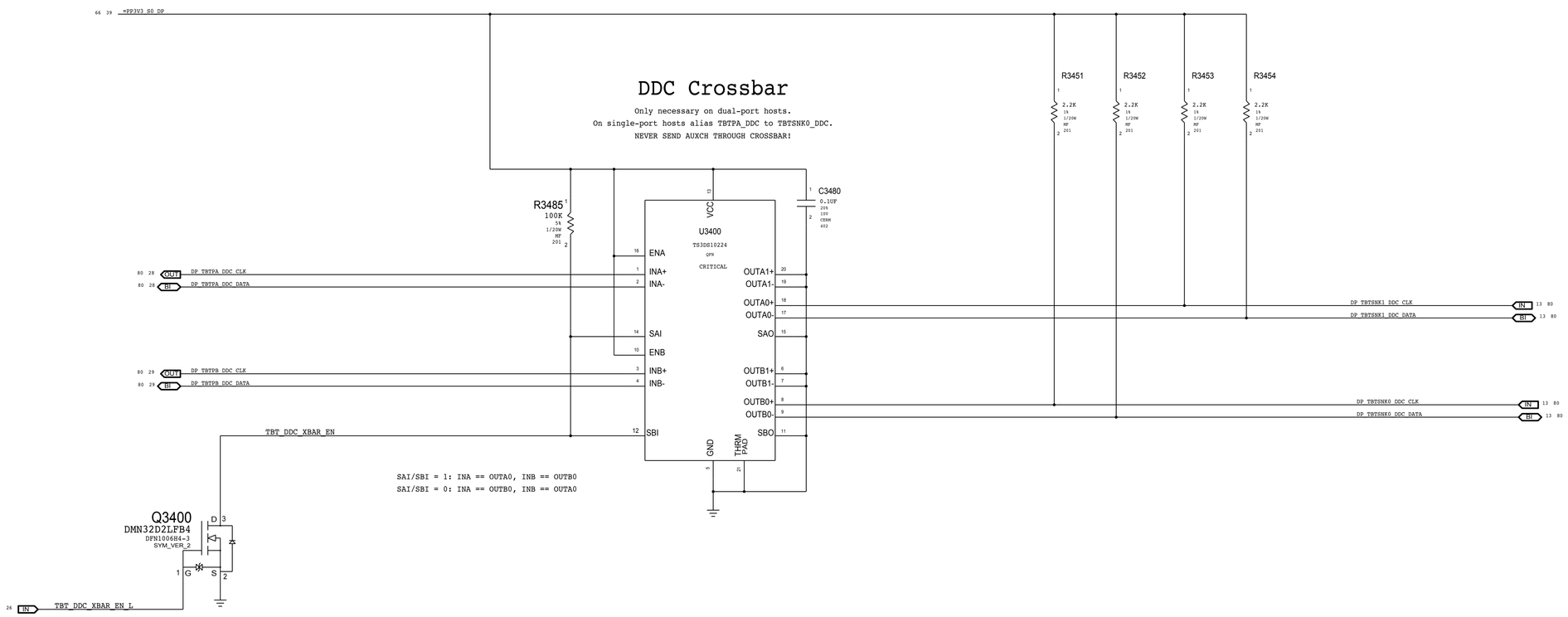
DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.



SYNC_MASTER=J70_TONY	SYNC_DATE=09/13/2013
PAGE TITLE: DDC Crossbar	
Apple Inc.	DRAWING NUMBER: 051-00081 — SIZE: D
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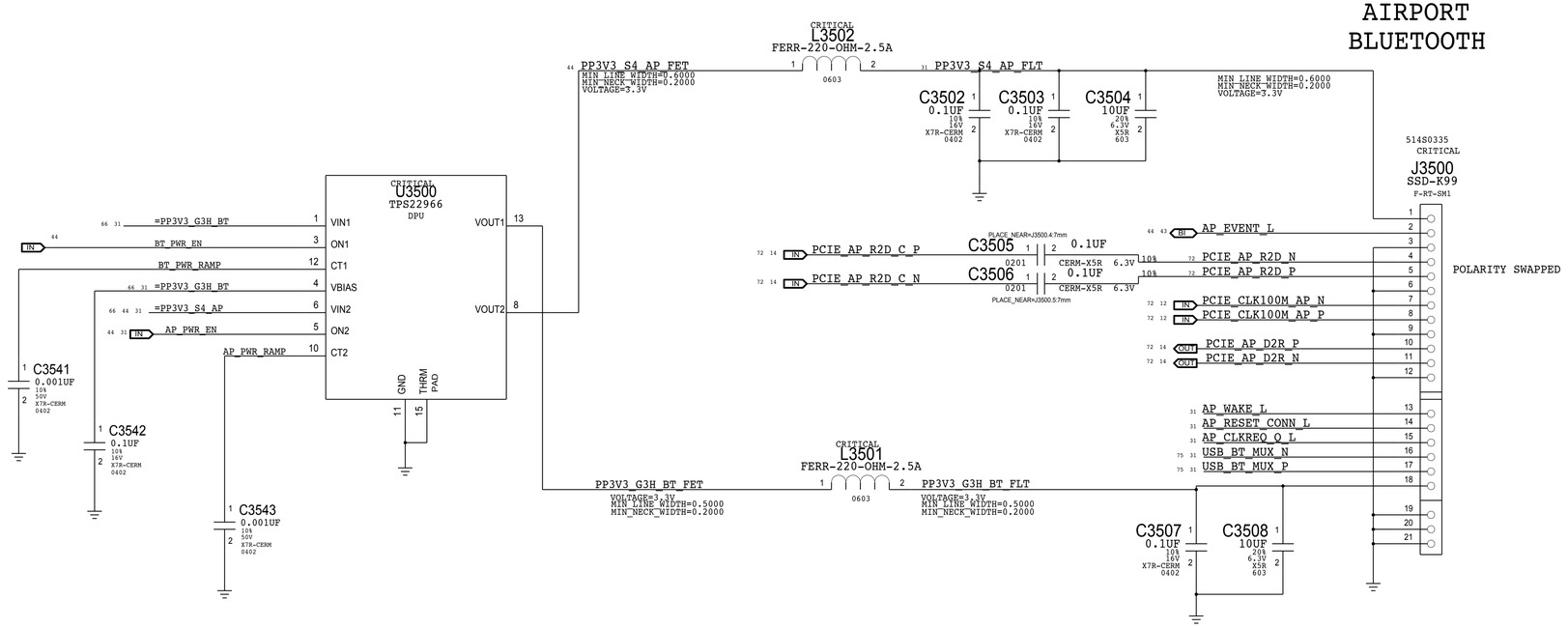
	SHEET: 30 OF 81

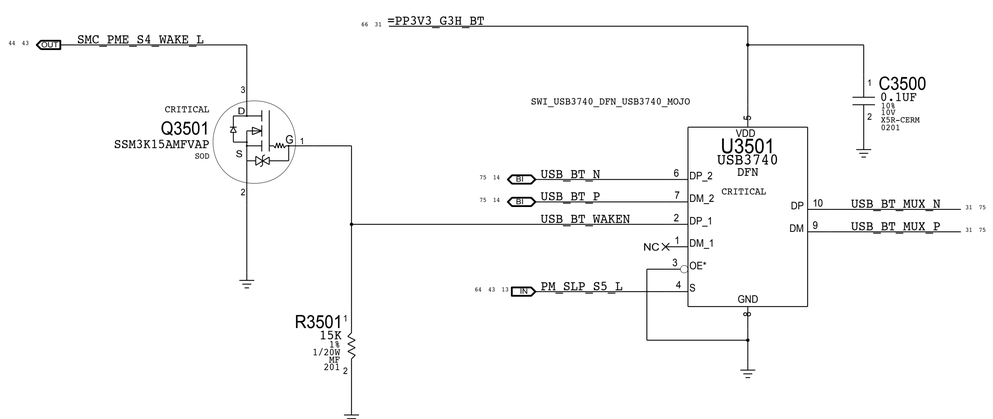
AIRPORT BLUETOOTH

AP & BT Load Switch

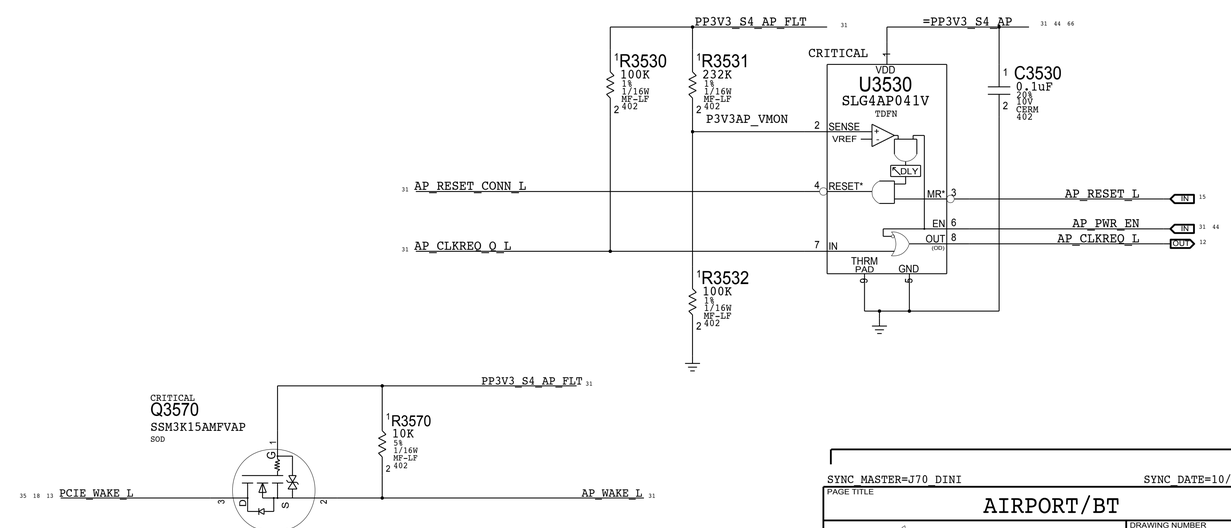
SWITCH	TPS22966
AP SLEW RATE	1185 us
BT SLEW RATE	1185 us
Equation	0.32*Ct + 13.7



Wake from BT in G3H circuit



Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%



SYNC_MASTER=J70_DINI SYNC_DATE=10/08/2013

PAGE TITLE: AIRPORT/BT

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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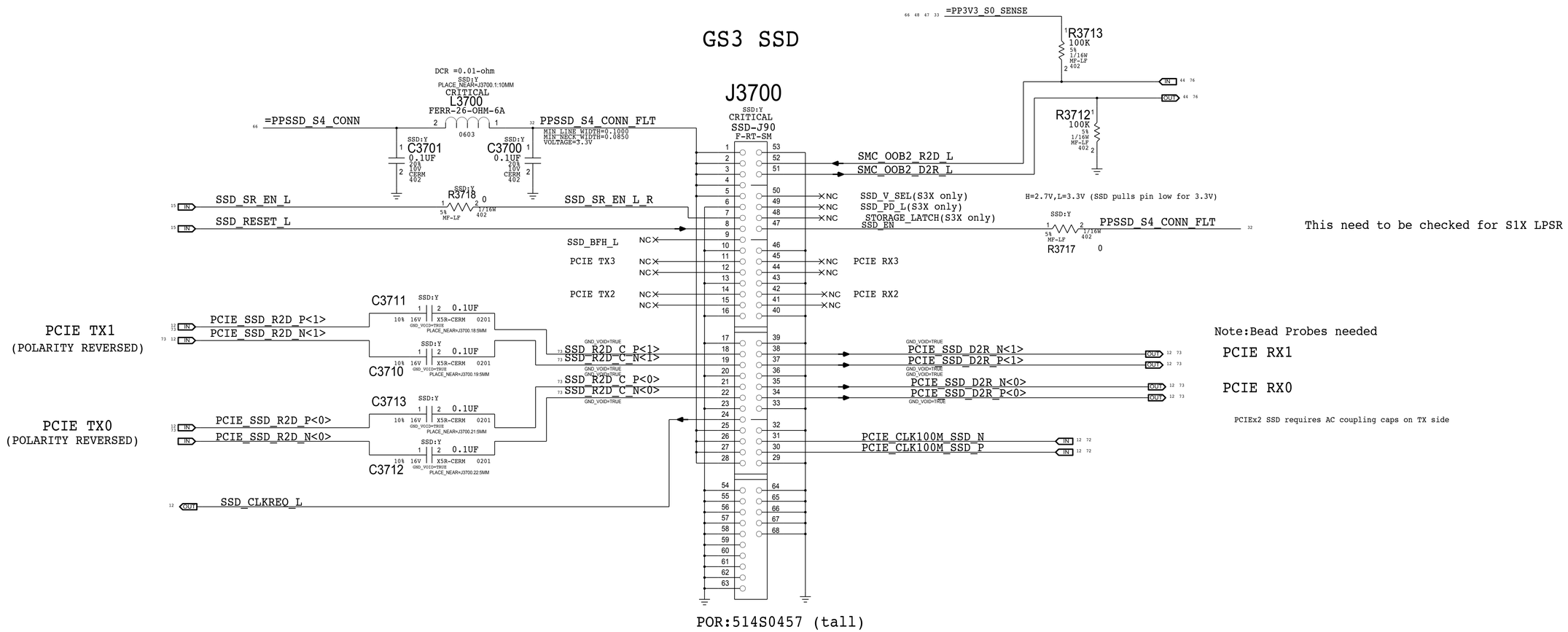
GS3 SSD



SYNC_MASTER=J70_DINI SYNC_DATE=10/14/2013

PAGE TITLE

SSD Connectors

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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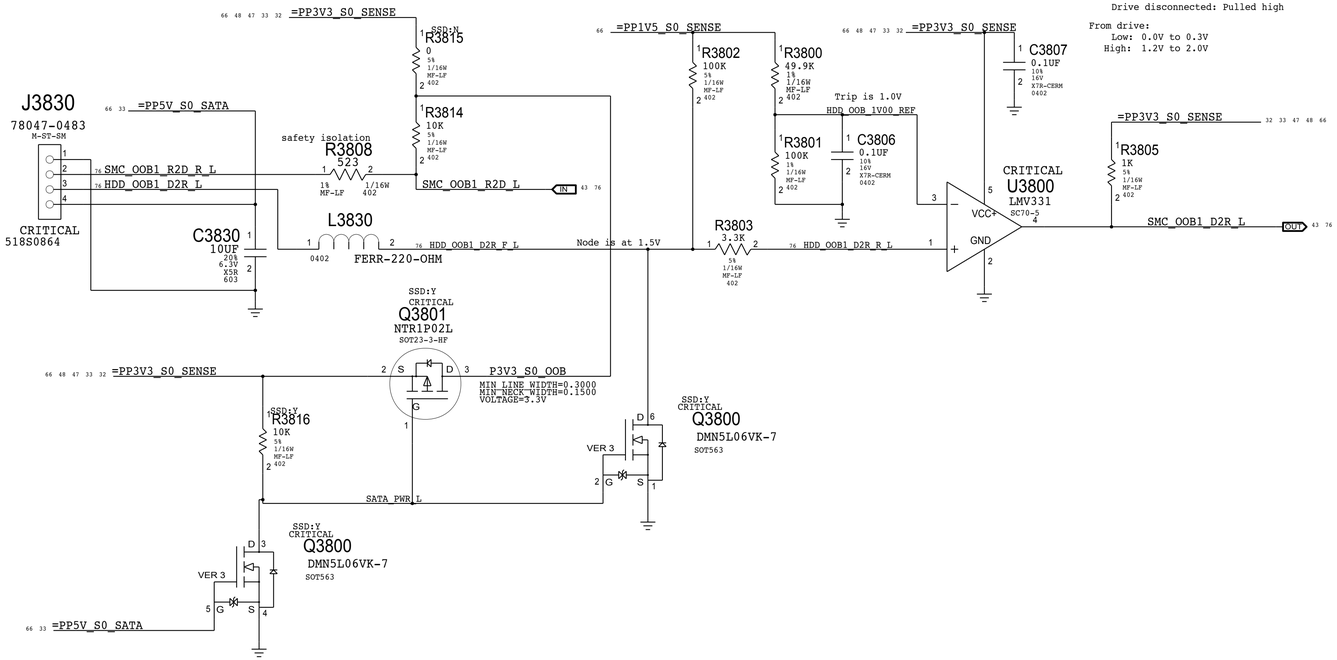
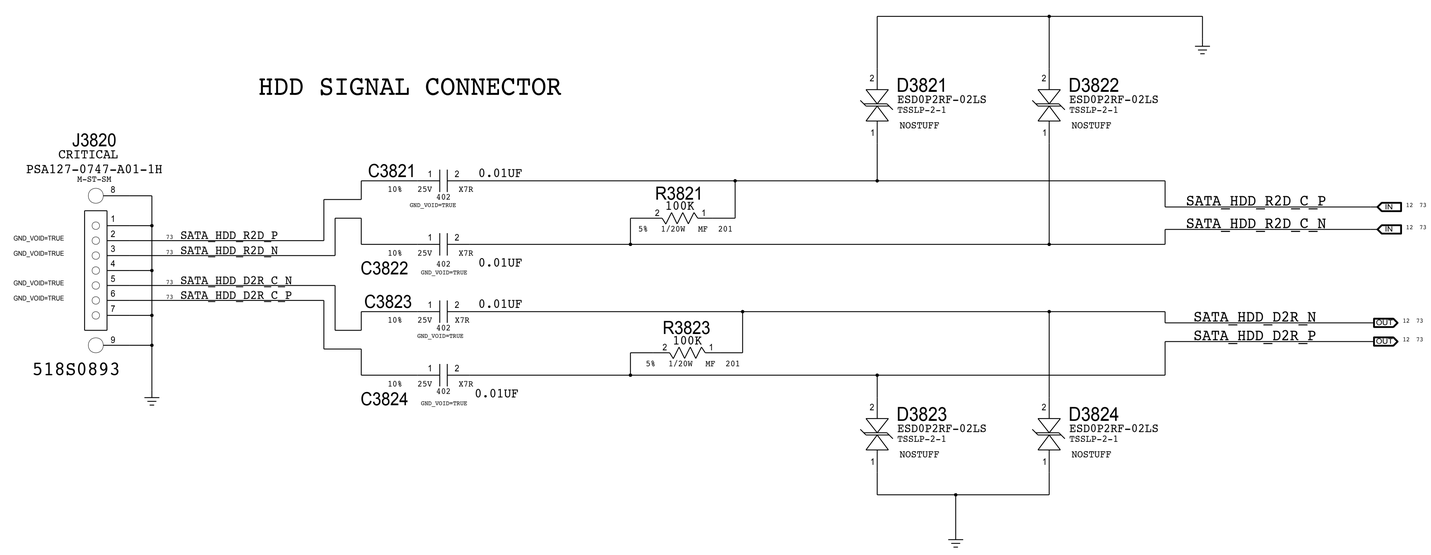
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing

Notes:
Drive active: Valid signal protocol
Drive asleep: HDD drives HDD_OOB_TEMP low
Drive disconnected: Pulled high
From drive:
Low: 0.0V to 0.3V
High: 1.2V to 2.0V



HDD SIGNAL CONNECTOR



SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: HDD Connector	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
	REVISION: 3.0.0
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO

CRITICAL L3900 FERR-600-OHM-300MA-0.850OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

Pin	Signal	Dir
58	VMAIN_PRSNT	(IPD-ENET)
27	PCIE_TXD_N	
28	PCIE_TXD_P	
33	PCIE_RXD_P	
34	PCIE_RXD_N	
31	PCIE_REFCLK_P	
30	PCIE_REFCLK_N	
11	PERST*	(IPD)
12	CLKREQ*	(OD)
3	WAKE*	(OD)
4	LOW_PWR	(IPD)
6	SMB_CLK	
10	SMB_DATA	(IPD-ENETM)
66	SCLK_SPD1000LED*	(IPU)
64	SI/EEDATA	(IPU)
65	SO_LINKLED*	(IPU)
63	CS*/EECLK	(IPU)
2	SPD100LED*/SERIAL_DO	(OD)
67	TRAFFICLED*/SERIAL_DI	(OD)
18	XTALI	
19	XTALO	
38	RDAC	
69	THRM_PAD	

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to strata.

ENET_VMAIN_PRSNT
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_TRAFFICLED_L
ENET_XTAL_IN
ENET_XTAL_OUT
ENET_RDAC
ENETSD_CLKREQ_L
ENET_LOW_PWR
ENET_RESET_L
R3965 1.24K 1% 1/16W MF-LF 402

Pin	Signal	Dir
40	TRD0_P	ENETCONN_MDI_P<0>
41	TRD0_N	ENETCONN_MDI_N<0>
44	TRD1_P	ENETCONN_MDI_P<1>
43	TRD1_N	ENETCONN_MDI_N<1>
46	TRD2_P	ENETCONN_MDI_P<2>
47	TRD2_N	ENETCONN_MDI_N<2>
50	TRD3_P	ENETCONN_MDI_P<3>
49	TRD3_N	ENETCONN_MDI_N<3>
5	GPIO_0/CR_ACT_LED*	NC
8	GPIO_1/LR_OUT	PP3V3R1V8_ENET_LR_OUT
9	GPIO_2/MEDIA_SENSE	ENET_MEDIA_SENSE
1	SD_DETECT	ENET_SD_DETECT_L
26	CR_CMD	ENET_SD_CMD
21	CR_CLK	ENET_SD_CLK
25	CR_DATA0	ENET_CR_DATA<0>
24	CR_DATA1	ENET_CR_DATA<1>
23	CR_DATA2	ENET_CR_DATA<2>
22	CR_DATA3	ENET_CR_DATA<3>
52	CR_DATA4	ENET_CR_DATA<4>
53	CR_DATA5	ENET_CR_DATA<5>
54	CR_DATA6	ENET_CR_DATA<6>
55	CR_DATA7	ENET_CR_DATA<7>
59	MS_INS*	NC
60	CR_LED*/CR_BUS_PWR	ENET_CR_PWREN
57	CR_WP*	SDCONN_WP
68	SR_DISABLE	ENET_SR_DISABLE

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
(See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

R3961 33 5% 1/20W MF 201
R3979 33 5% 1/20W MF 201
R3971 33 5% 1/20W MF 201
R3972 33 5% 1/20W MF 201
R3973 33 5% 1/20W MF 201
R3974 33 5% 1/20W MF 201
R3975 33 5% 1/20W MF 201
R3976 33 5% 1/20W MF 201
R3977 33 5% 1/20W MF 201
R3978 33 5% 1/20W MF 201
R3981 1K 5% 1/16W MF-LF 402

SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3R1V8_CR_VDDIO
C3980 4.7UF 20% 6.3V X5R-CERM1 402
C3981 0.1UF 10% 16V X5R-CERM 0201
C3982 0.1UF 10% 16V X5R-CERM 0201

ENET_MEDIA_SENSE
ENET_SD_DETECT_L
ENET_SR_DISABLE

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

ENET supports both active-levels for WP.

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC, SCK, CS*, WP*, RESET*, SI, SO, GND
ENET_SCLK, ENET_CS_L, ENET_MOSI, ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J70_GAREN SYNC_DATE=09/19/2013
PAGE TITLE: ETHERNET PHY (CAESAR IV)
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DRAWING NUMBER 051-00081 SIZE D
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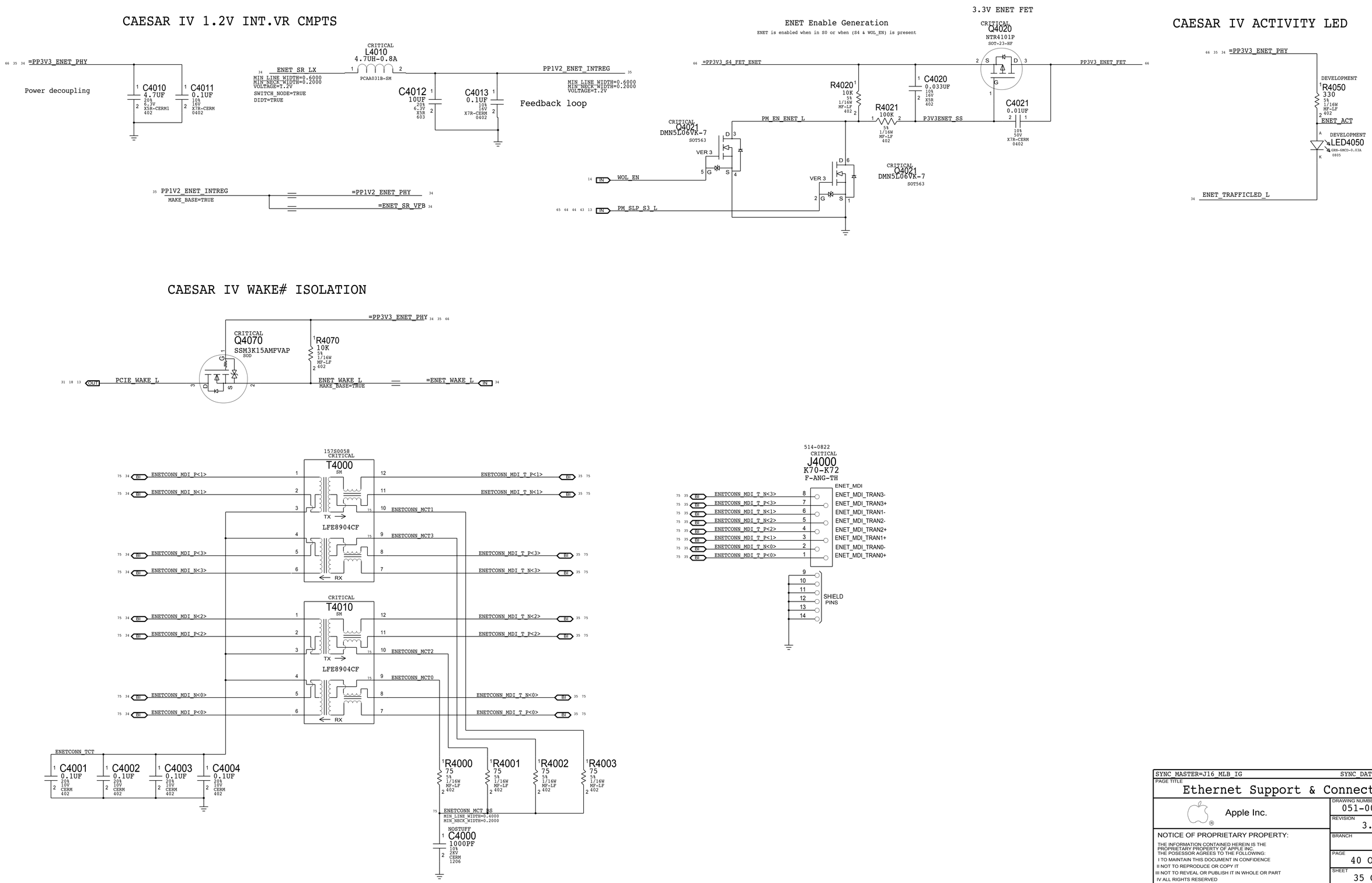

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE
Ethernet Support & Connector

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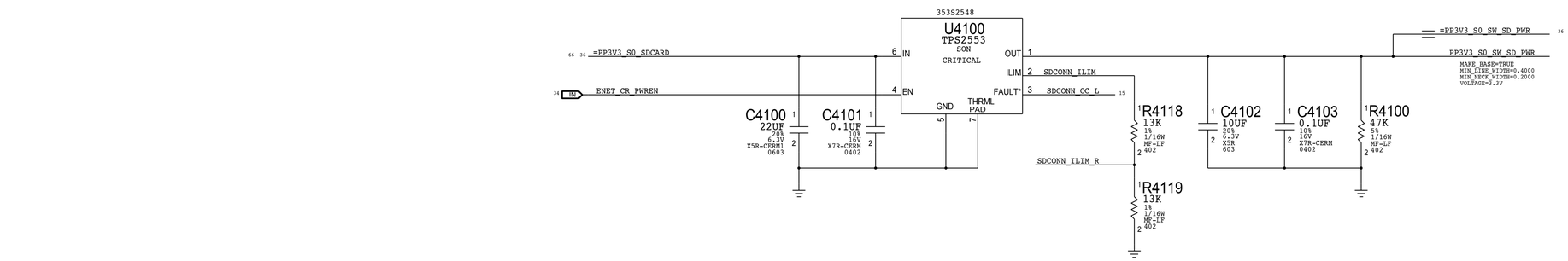
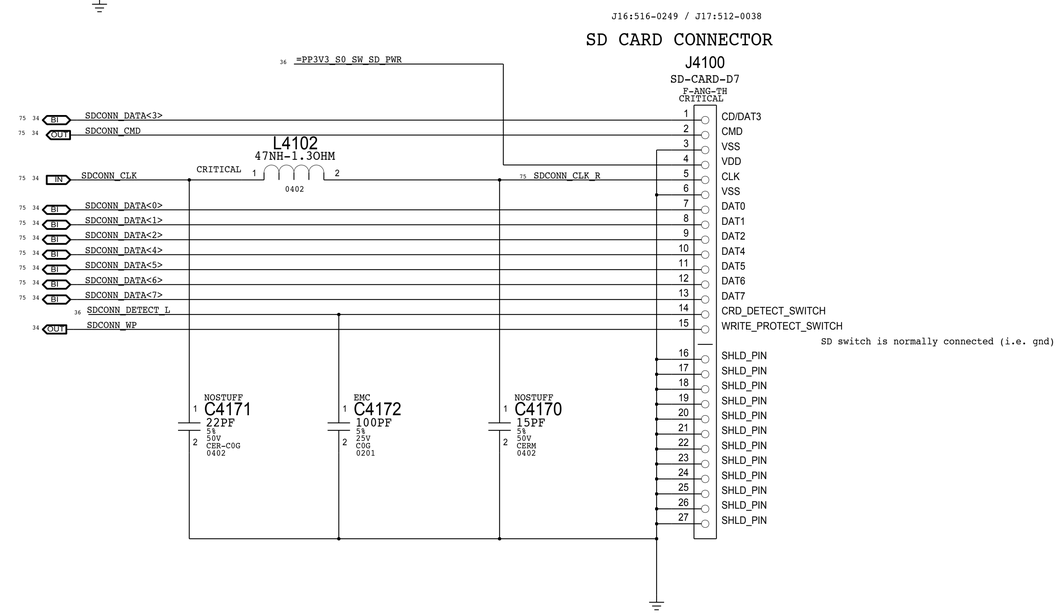
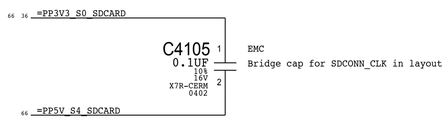
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

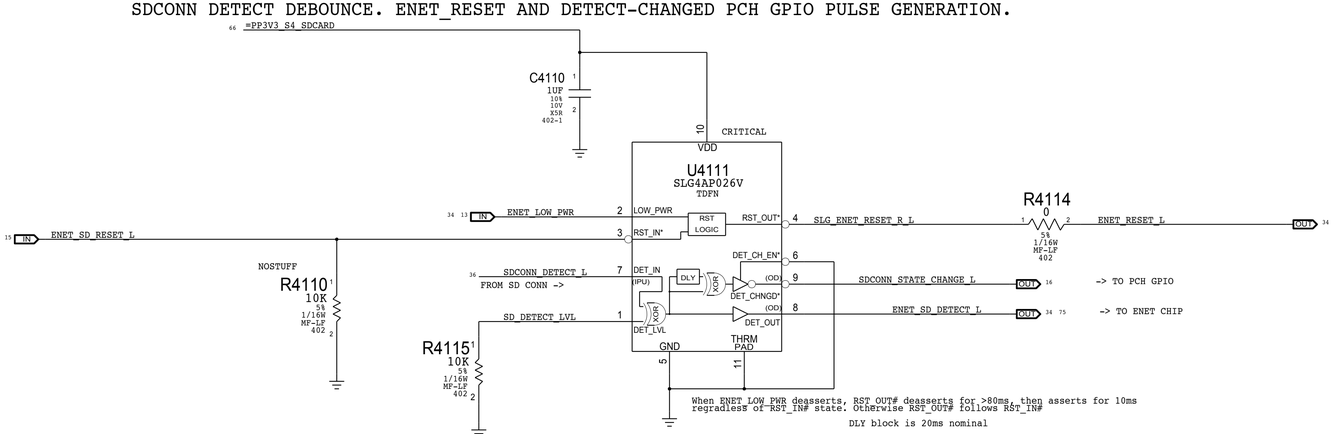


SD CARD CONNECTOR





SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J70_GAREN	SYNC_DATE=09/23/2013
PAGE TITLE: SD READER CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
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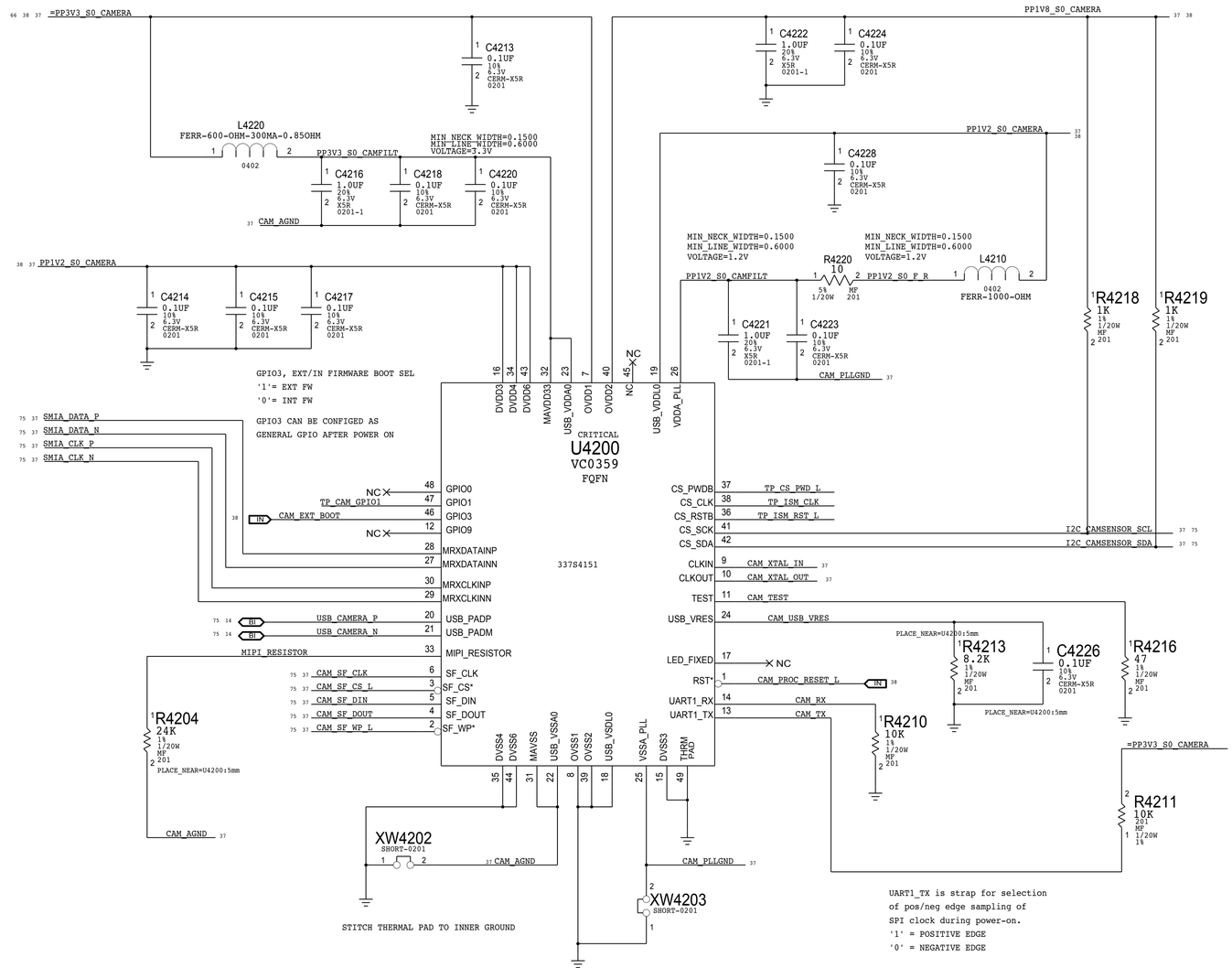
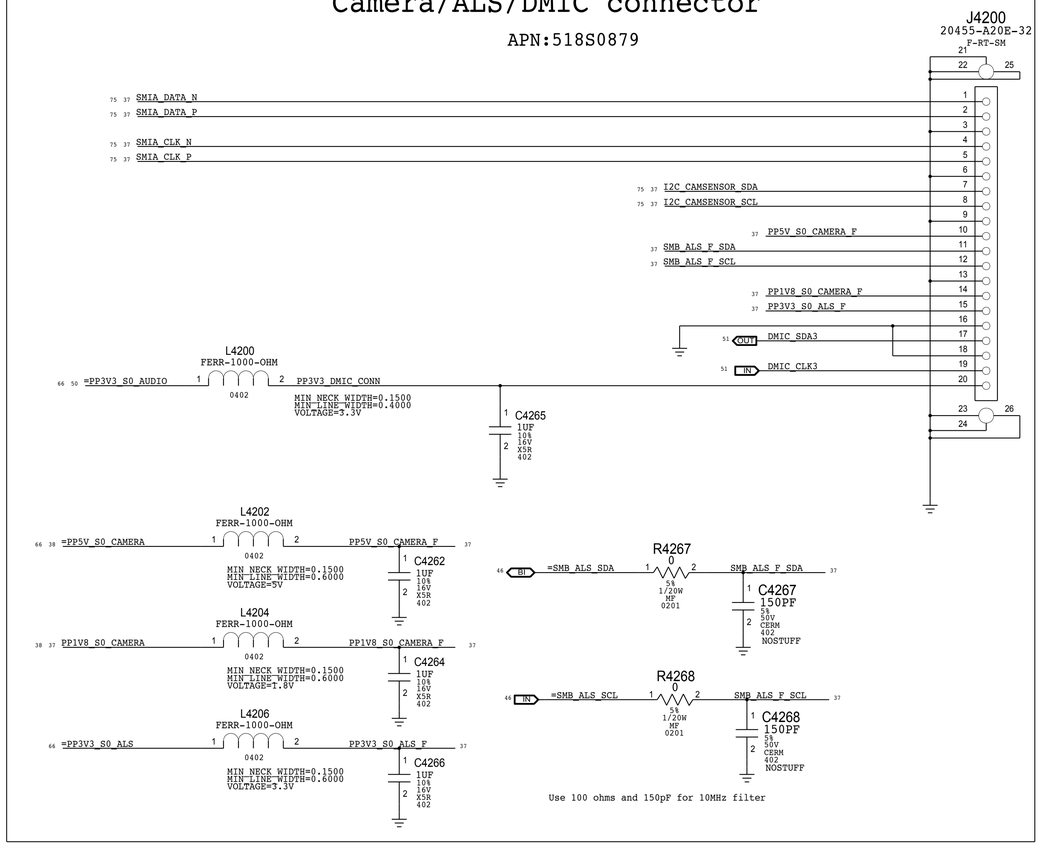
USB CAMERA CONTROLLER

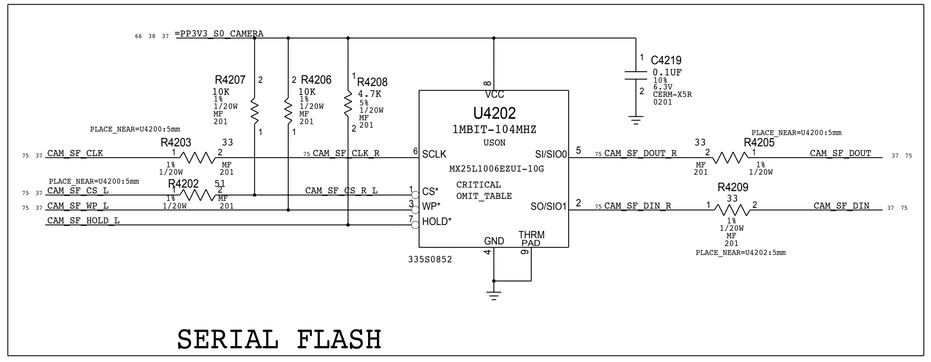


Camera/ALS/DMIC connector

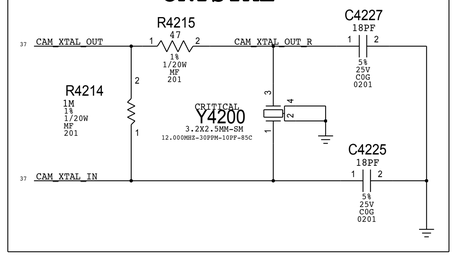
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J70_GAREN	SYNC_DATE=02/05/2014
PAGE TITLE: Camera Controller	
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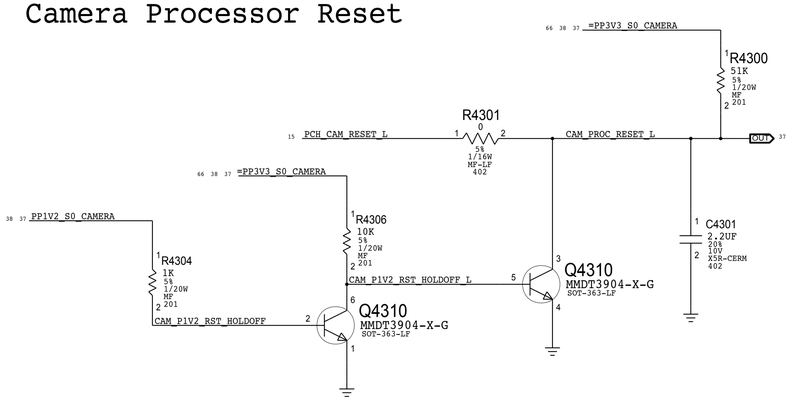
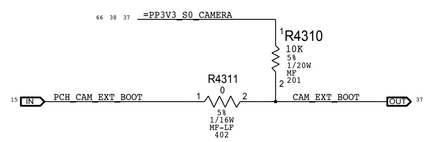
Camera Processor Reset

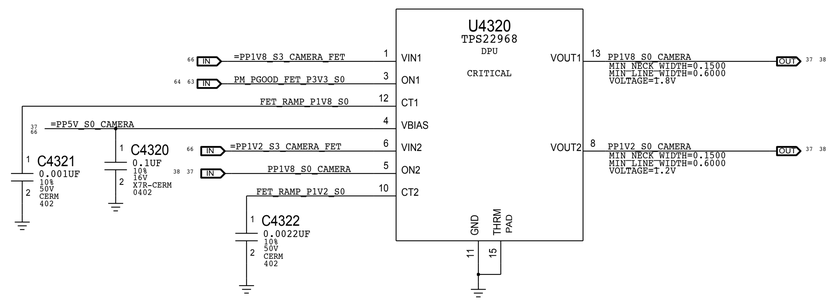


Camera Processor ExtBoot Cntl



1.8V S0 and 1.2V S0 Load Switch

POWER SEQUENCE
3.3V => 1.8V => 1.2V
Enable 1.8V camera rail when 3.3V S0 rail is on
Enable 1.2V camera rail when 1.8V S0 rail is on



Capacitor Values Found Using
Slew Rate(us/V) = 0.32*CT(pF) + 13.7

Rise Times:
1.8V S0 -- 1000 pF -- 600 us
1.2V S0 -- 2200 pF -- 861 us

SYNC_MASTER=J70_GAREN SYNC_DATE=10/24/2013

PAGE TITLE
Camera Controller Support

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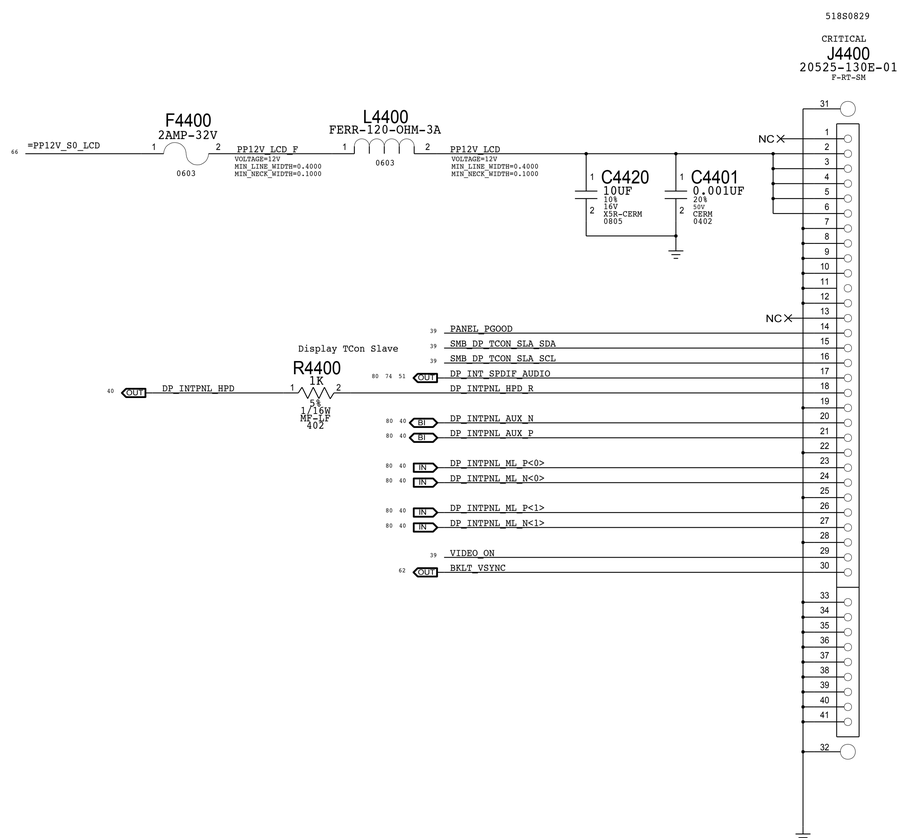
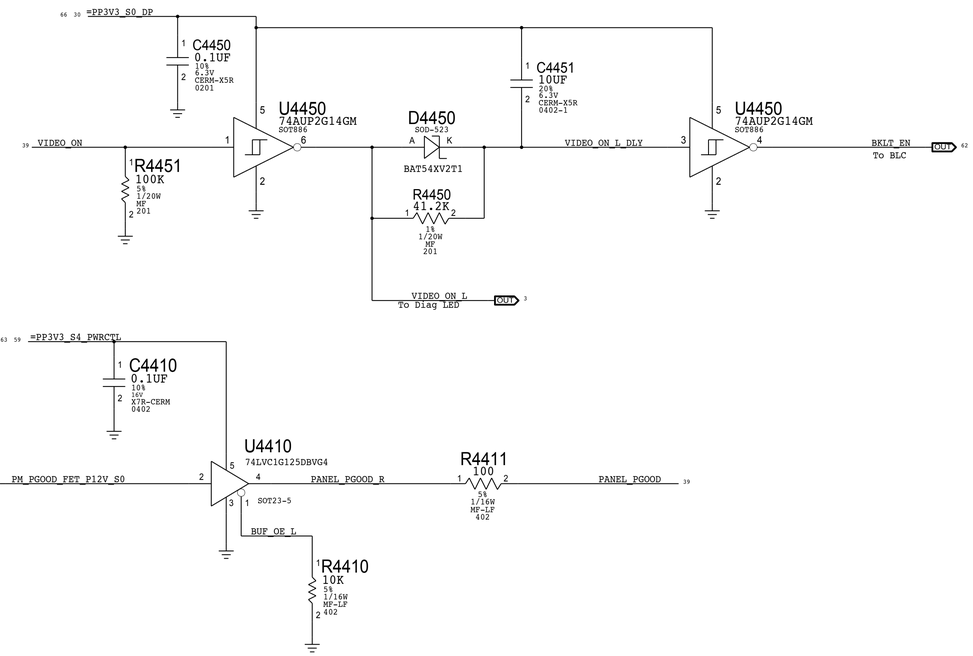
Internal DP Connector

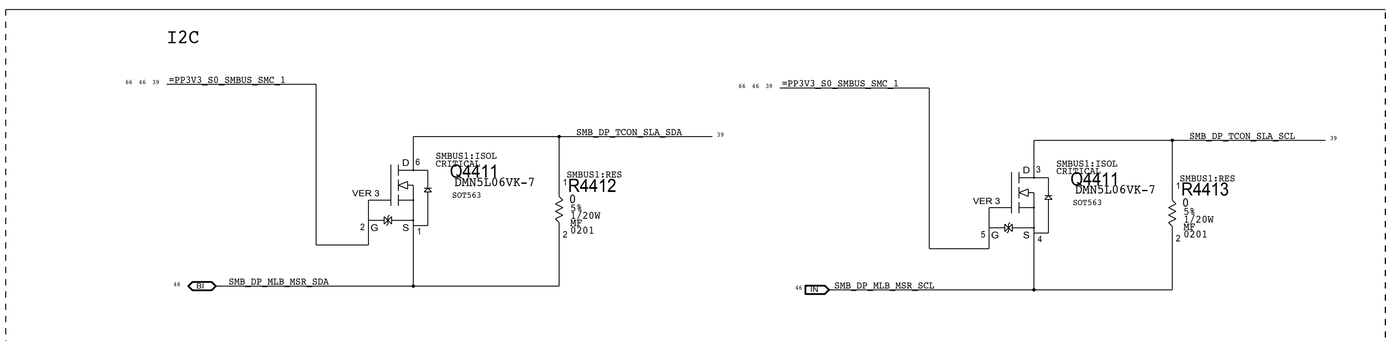


Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video



SMBus Isolation



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
Internal DP Support

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DRAWING NUMBER 051-00081 SIZE D
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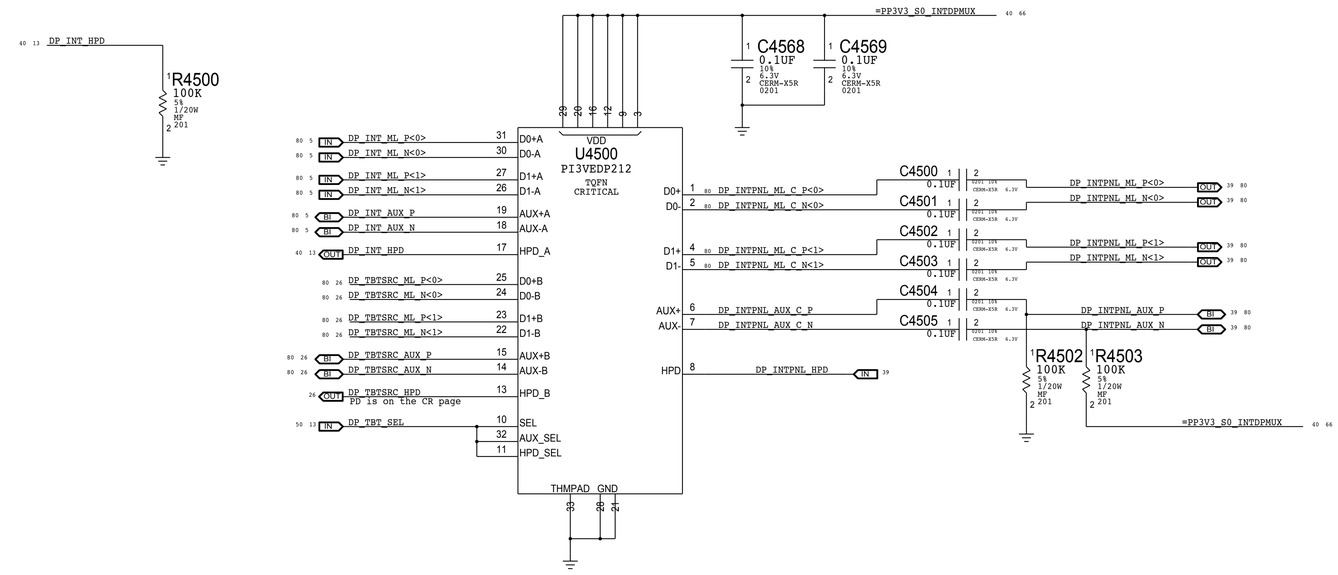
NC aliases

26 IN	DP_TBTSRC_ML_P<2>	NC_DP_TBTSRC_ML_P<2>	NO_TEST=1 MAKE_BASE=TRUE
26 IN	DP_TBTSRC_ML_N<2>	NC_DP_TBTSRC_ML_N<2>	NO_TEST=1 MAKE_BASE=TRUE
26 IN	DP_TBTSRC_ML_P<3>	NC_DP_TBTSRC_ML_P<3>	NO_TEST=1 MAKE_BASE=TRUE
26 IN	DP_TBTSRC_ML_N<3>	NC_DP_TBTSRC_ML_N<3>	NO_TEST=1 MAKE_BASE=TRUE
5 IN	DP_INT_ML_P<2>	NC_DP_INT_ML_P<2>	NO_TEST=1 MAKE_BASE=TRUE
5 IN	DP_INT_ML_N<2>	NC_DP_INT_ML_N<2>	NO_TEST=1 MAKE_BASE=TRUE
5 IN	DP_INT_ML_P<3>	NC_DP_INT_ML_P<3>	NO_TEST=1 MAKE_BASE=TRUE
5 IN	DP_INT_ML_N<3>	NC_DP_INT_ML_N<3>	NO_TEST=1 MAKE_BASE=TRUE



SYNC_MASTER=J70_TONY SYNC_DATE=09/05/2013

PAGE TITLE

Internal DP MUXing

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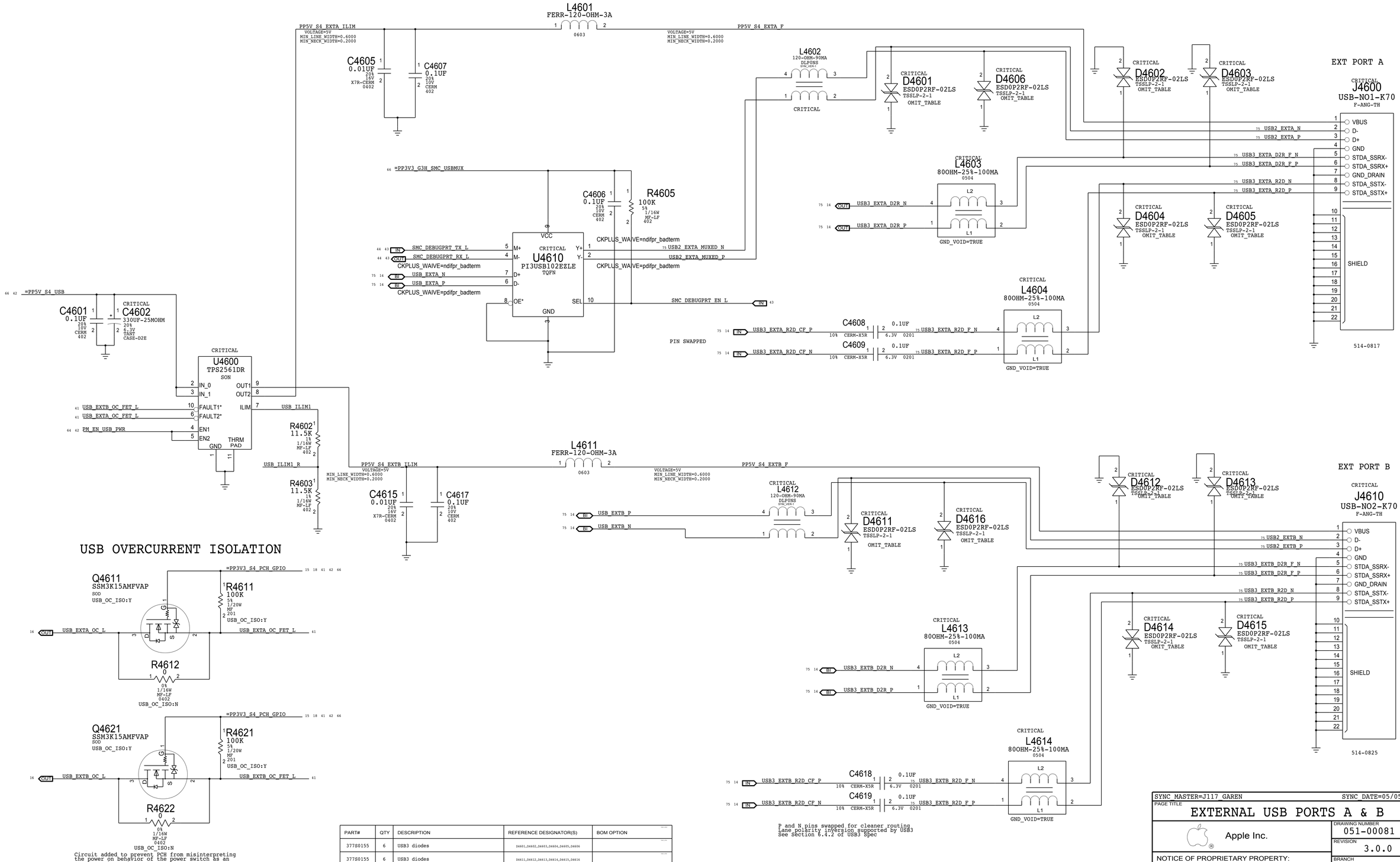

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S0155	6	USB3 diodes	D4601,D4602,D4603,D4604,D4605,D4606	
377S0155	6	USB3 diodes	D4611,D4612,D4613,D4614,D4615,D4616	

SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE
EXTERNAL USB PORTS A & B

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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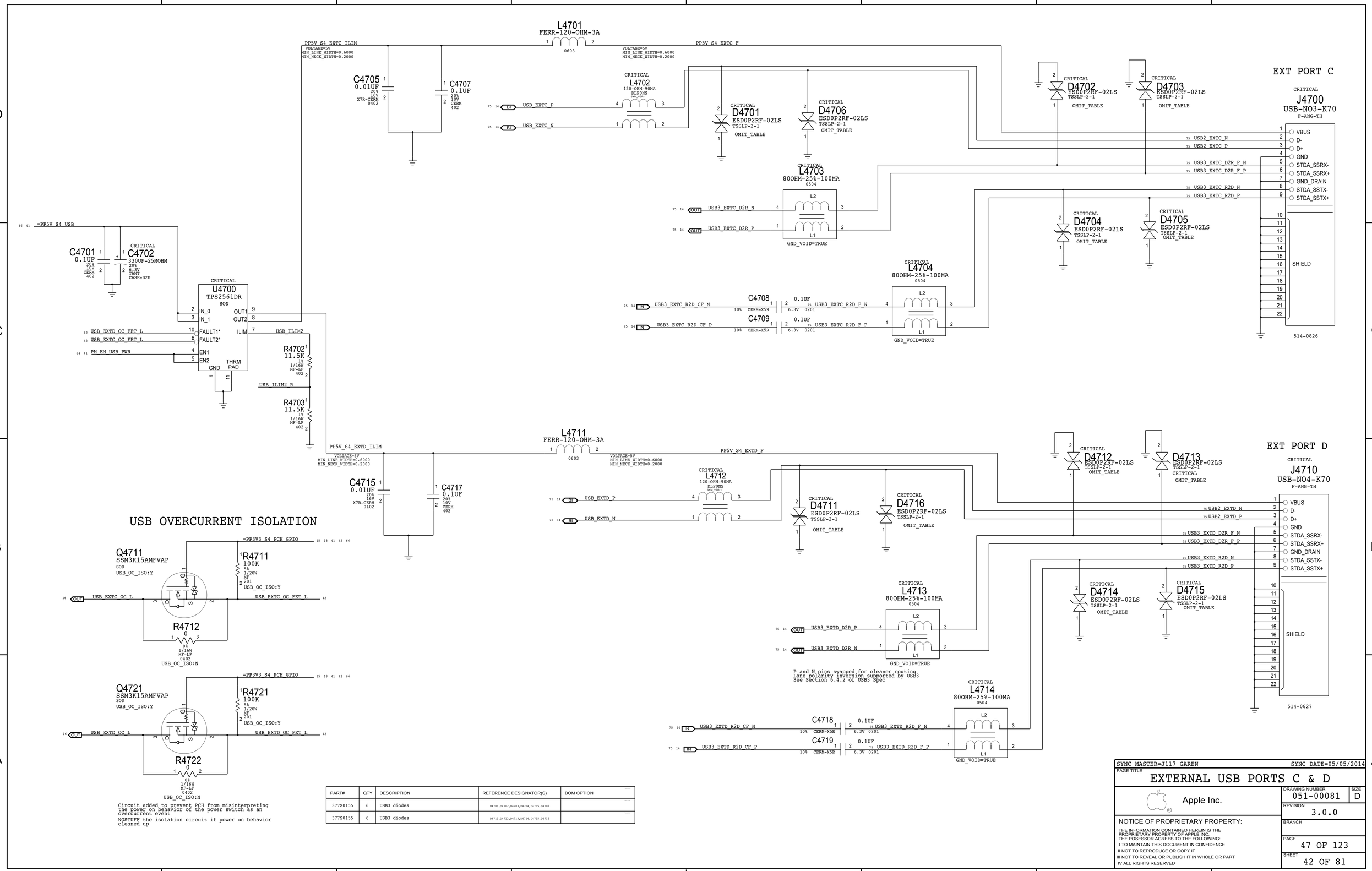

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S0155	6	USB3 diodes	D4701,D4702,D4703,D4704,D4705,D4706	
377S0155	6	USB3 diodes	D4711,D4712,D4713,D4714,D4715,D4716	

SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE

EXTERNAL USB PORTS C & D

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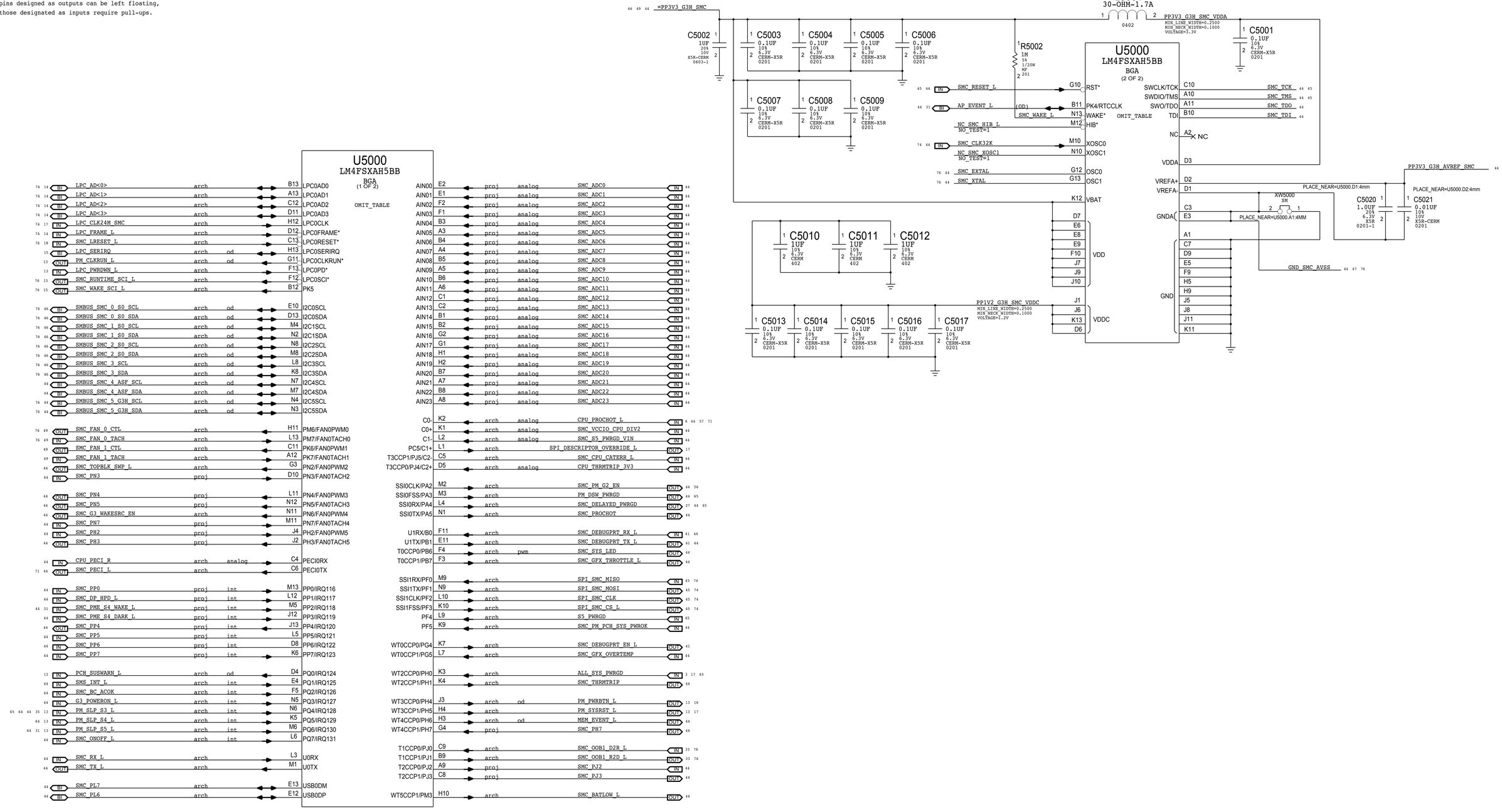
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SYNC_MASTER=J70_NICK	SYNC_DATE=09/24/2013
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-00081 — SIZE: D
	REVISION: 3.0.0
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	PAGE: 50 OF 123
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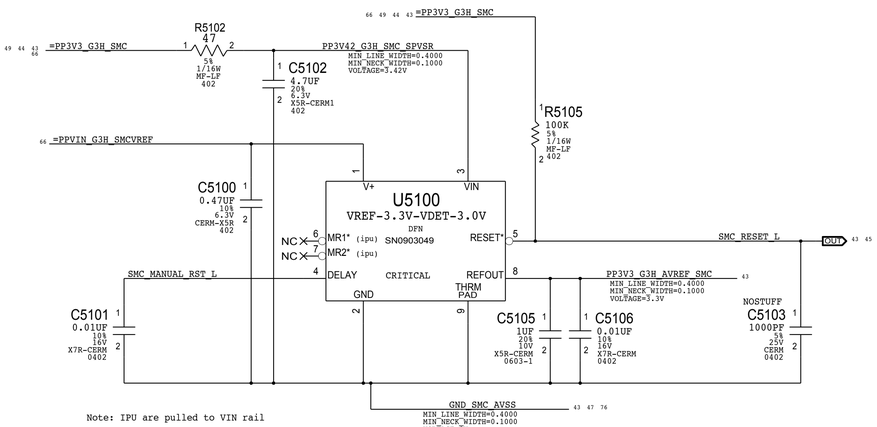
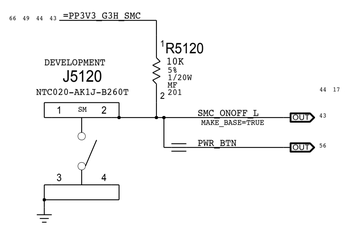
SMC Supervisor and AVREF Supply



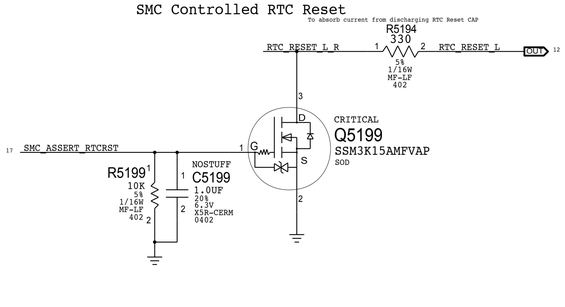
Note: IPU are pulled to VIN rail

Power Button

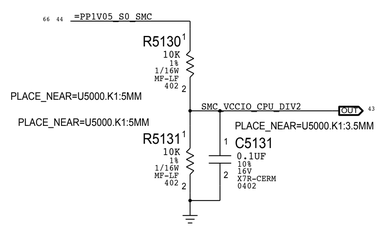


SMC Controlled RTC Reset

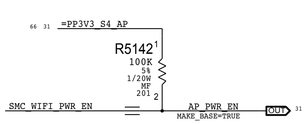
To absorb current from discharging RTC Reset CAP



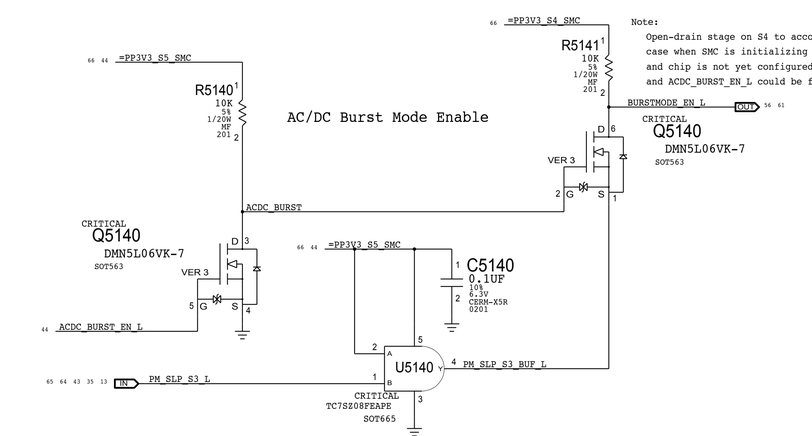
Comparator Reference



SMC control for AirPort power



AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC6	VSNS_P1V2_S3_DDR	MAKE_BASE=TRUE
SMC_ADC7	ISNS_P1V2_S3_DDR	MAKE_BASE=TRUE
SMC_ADC10	VSNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC11	ISNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC20	VSNS_P3V3_SSD	MAKE_BASE=TRUE
SMC_ADC21	ISNS_SSDS4	MAKE_BASE=TRUE

Unused ADC Channels

SMC_ADC2	NC_VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC3	NC_ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC4	NC_VSNS_PVDDQS0	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC5	NC_ISNS_PVDDQS0	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC8	NC_VSNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC9	NC_ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC12	NC_VSNS_GPUCORE_ALT	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC13	NC_ISNS_GPUCORE_ALT	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC14	NC_VSNS_HDDS0	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC15	NC_ISNS_HDDS0	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC16	NC_SMC_ADC16	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC17	NC_SMC_ADC17	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC18	NC_VSNS_P1V05S0_PCH	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC19	NC_ISNS_P3V3S4_AP	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE	NO_TEST=1

Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE
SMC_PH3	SMC_PCH_SUSACK_L	MAKE_BASE=TRUE
SMC_PL7	BT_PWR_EN	MAKE_BASE=TRUE

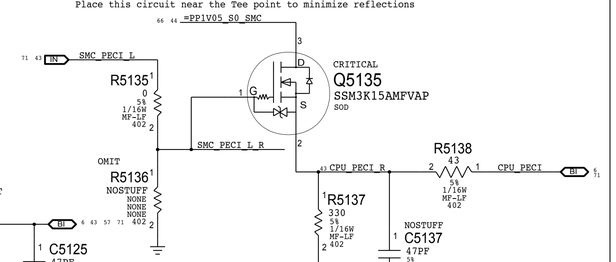
Unused Project-specific

SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=1
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PH7	NC_SMC_PH7	MAKE_BASE=TRUE	NO_TEST=1
TP for access if ZPB re-intstated			
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	NO_TEST=1
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE	NO_TEST=1
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE	NO_TEST=1
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE	NO_TEST=1
SMC_BATLOW_L	NC_SMC_BATLOW_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1
MEM_EVENT_L	NC_MEM_EVENT_L	MAKE_BASE=TRUE	NO_TEST=1

Platform Thermal Control

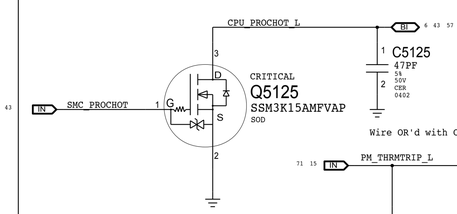
PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections

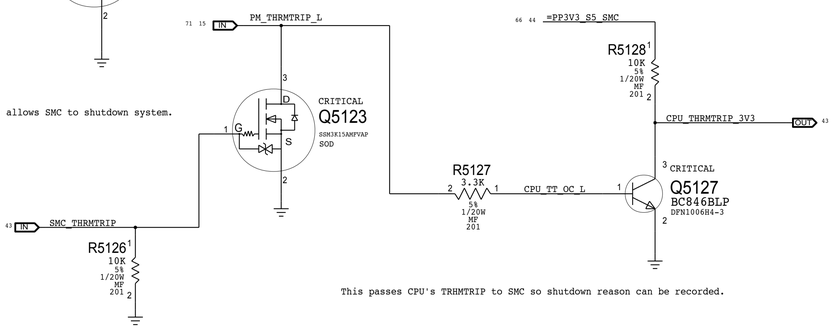


PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT



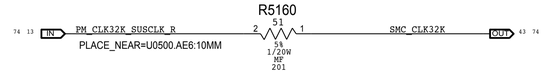
Wire OR'd with CPU



This allows SMC to shutdown system.

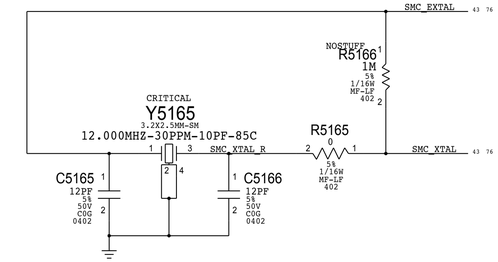
This passes CPU's TRHMTRIP to SMC so shutdown reason can be recorded.

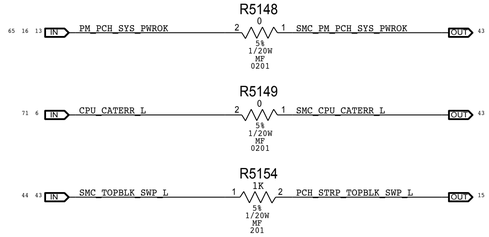
SMC 32KHz Clock



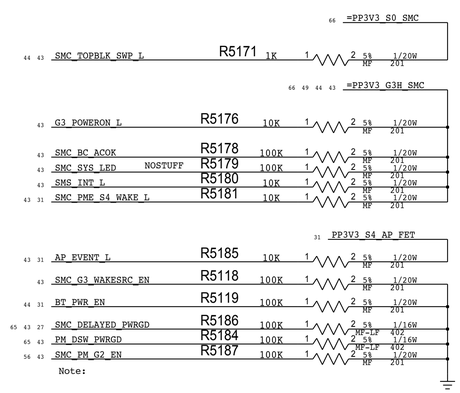
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



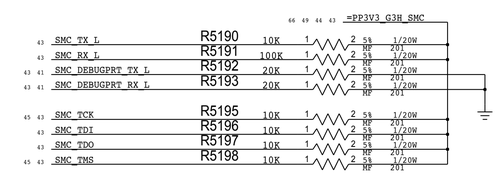


Arch Pull Up/Down



Note:

Serial/JTAG Interface Pull-ups



SYNC_MASTER=J70_NICK SYNC_DATE=01/15/2014

PAGE TITLE
SMC Support

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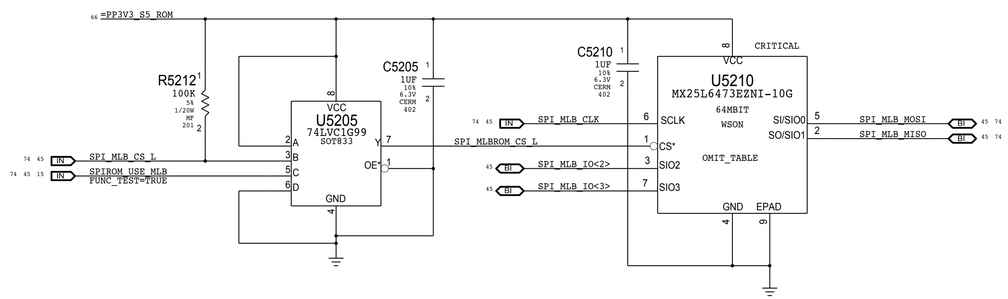
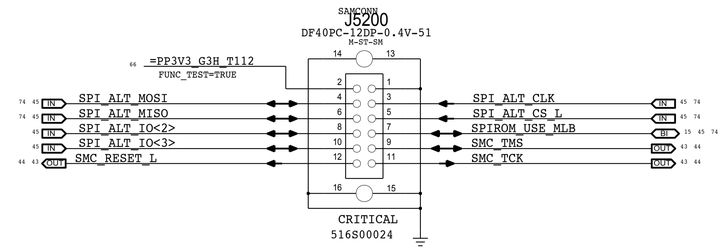
SPI BootROM

Quad_IO Mode (Mode 0 & 3) supported
SPI Freq: 50MHz for PCH, 20 MHz for SMC

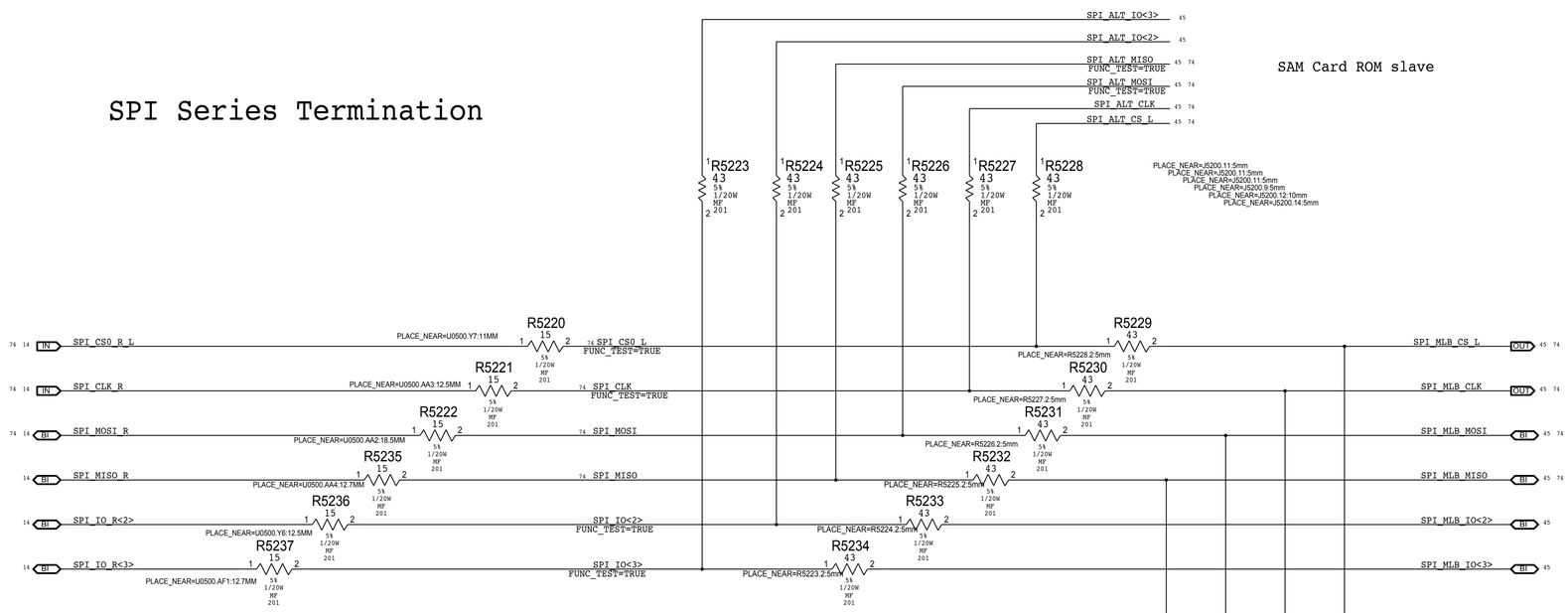


SPI+SWD SAM Connector

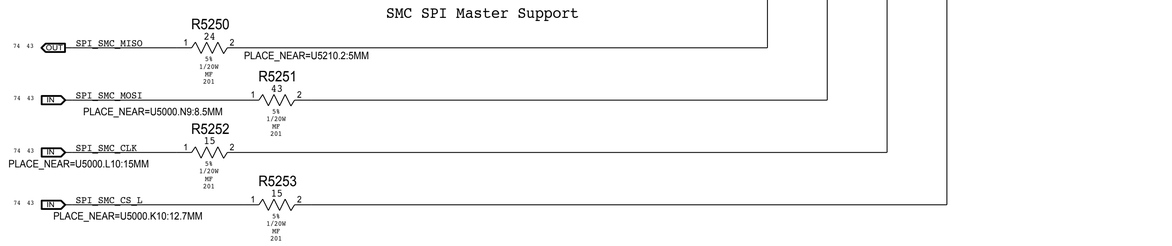


SPI Series Termination

SAM Card ROM slave



SMC SPI Master Support



SYNC MASTER=J117_TONY SYNC DATE=05/05/2014

PAGE TITLE
SPI and Debug Connector

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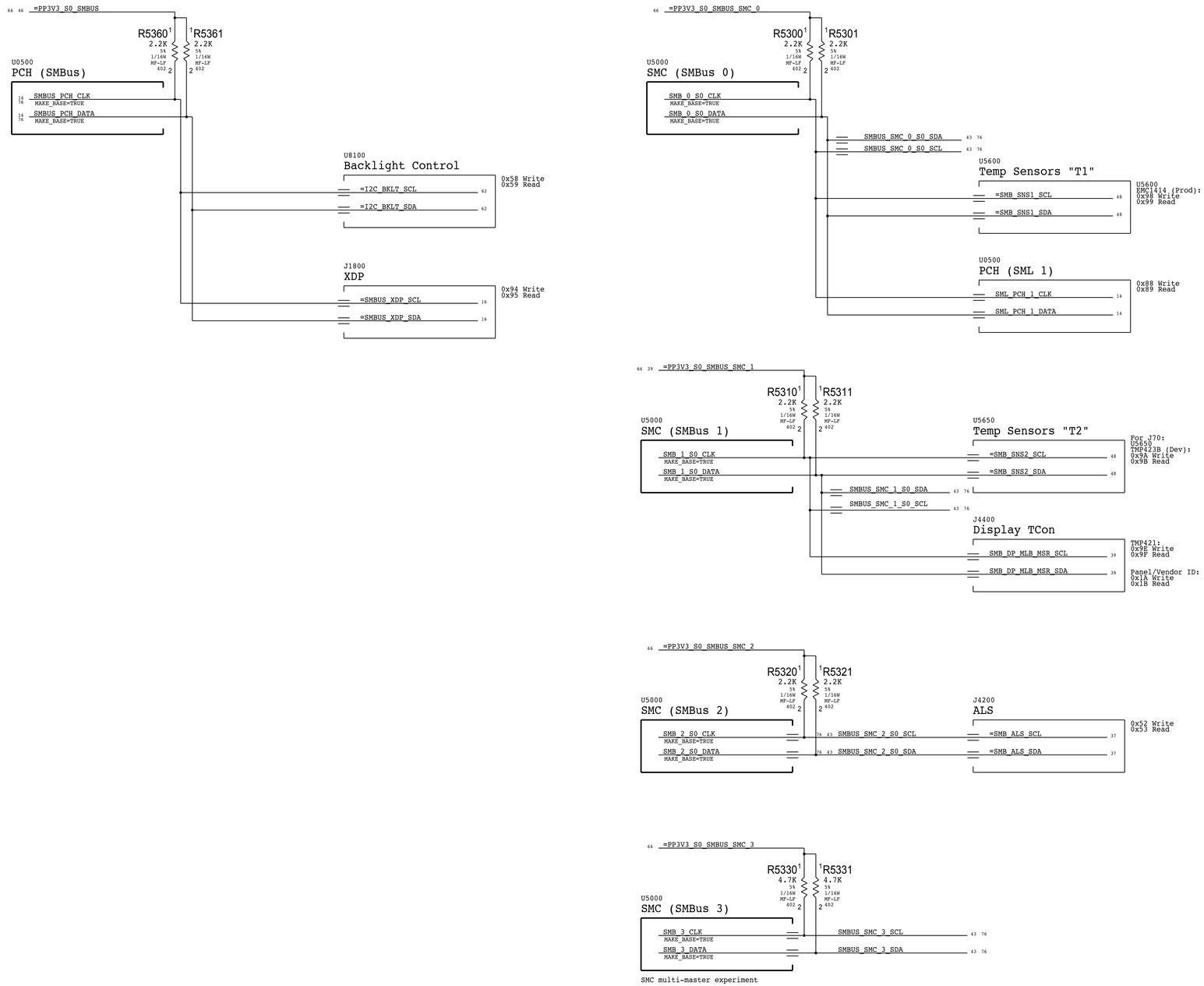

SYNC_MASTER=J70_NICK SYNC_DATE=02/14/2014

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SMBus Connections

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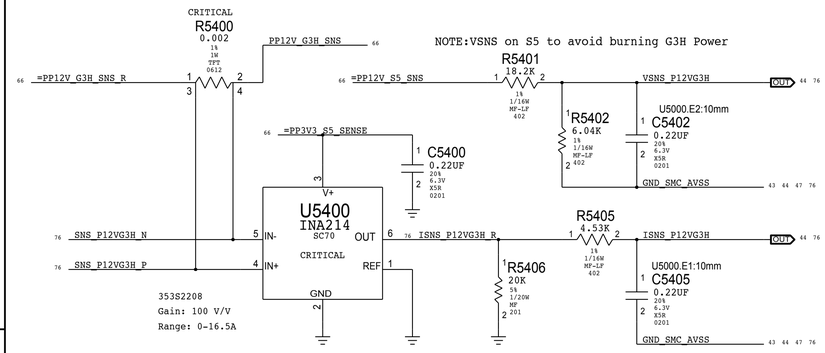
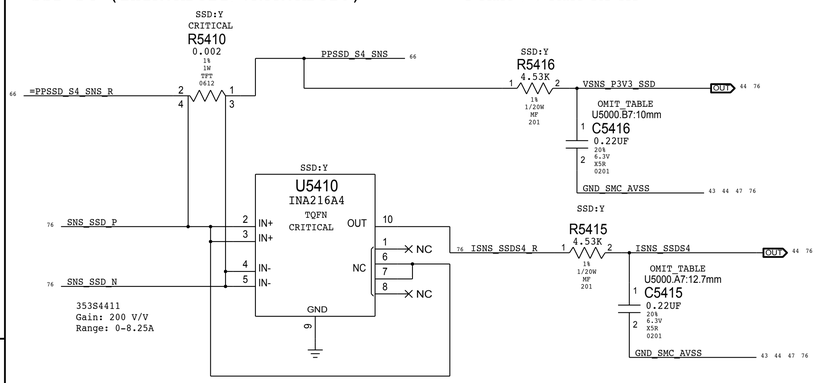
12V G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



SSD S4 (IH1R:ADC21/VR3R:ADC20)

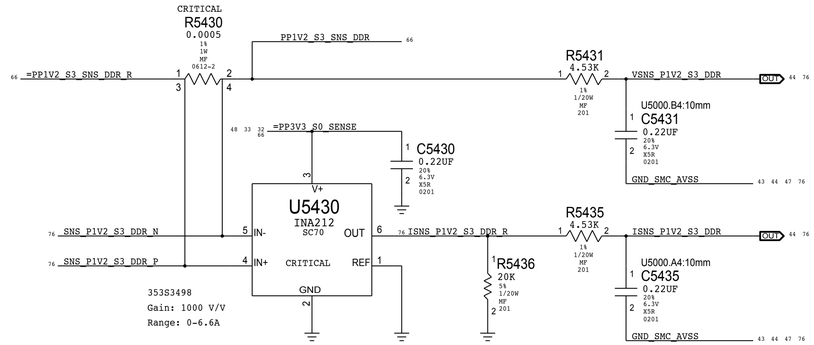
I-sense / V-sense for SSD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280304	2	CAP,0.22UF,201	C5415,C5416	SSD:Y
11780201	2	RES,0 OHM,201	C5415,C5416	SSD:N

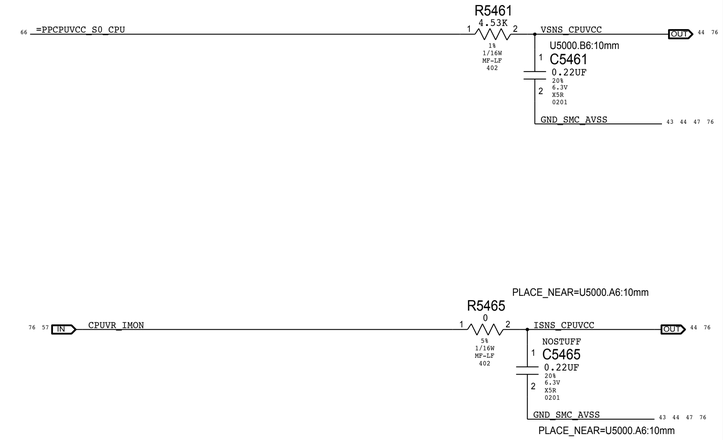
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for DDR



CPU Core (VC0C:ADC10/IC0C:ADC11)

Voltage sense and IMON amp (VC0C, IC0C)



SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE

I and V Sense

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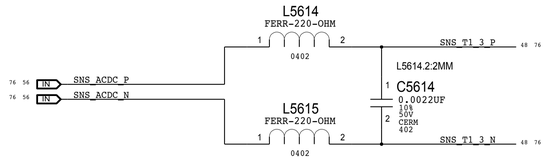
Temperature Sensor T1

LPDDR3 Proximity

PLACEMENT_NOTE=Place Q5610 between U2400 and U2500

AC/DC

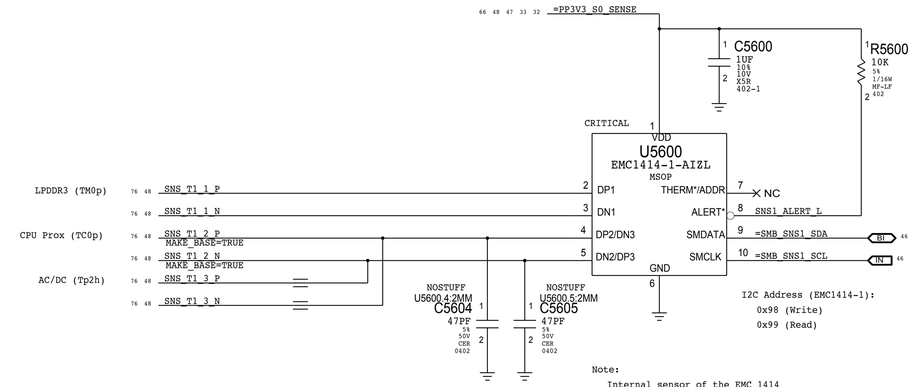
Diode on supply



CPU Proximity

PLACEMENT_NOTE=Place Q5612 underneath CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



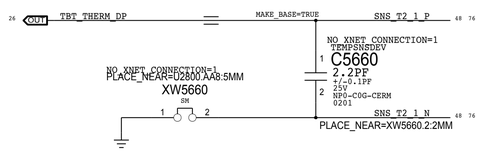
I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

Filter Caps: Stuff if needed for PSU sensor SI

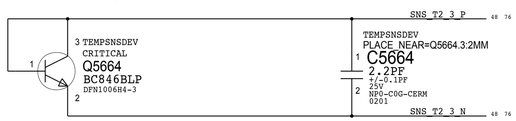
Note:
Internal sensor of the EMC 1414
will be used as the ambient sensor.
Place U5600 at the coolest location
on the MLB.

Temperature Sensor T2

TBT On Die

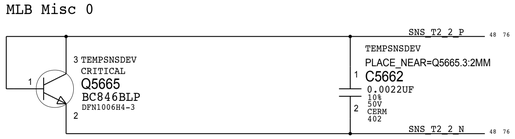


BLC Proximity

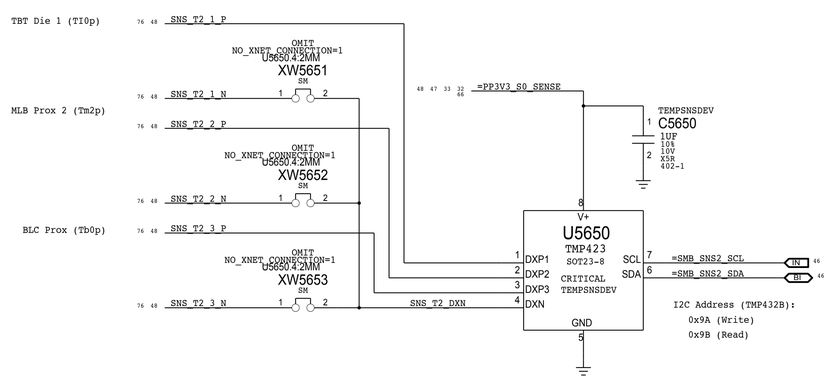


PLACEMENT_NOTE=Place Q5664 near BLC controller

MLB Misc 0



PLACEMENT_NOTE=PLACE Q5665 near CPU



I2C Address (TMP432B):
0x9A (Write)
0x9B (Read)

SYNC_MASTER=J70_NICK	SYNC_DATE=11/05/2013
PAGE TITLE: Temperature Sensors	
Apple Inc.	DRAWING NUMBER: 051-00081 / SIZE: D
	REVISION: 3.0.0
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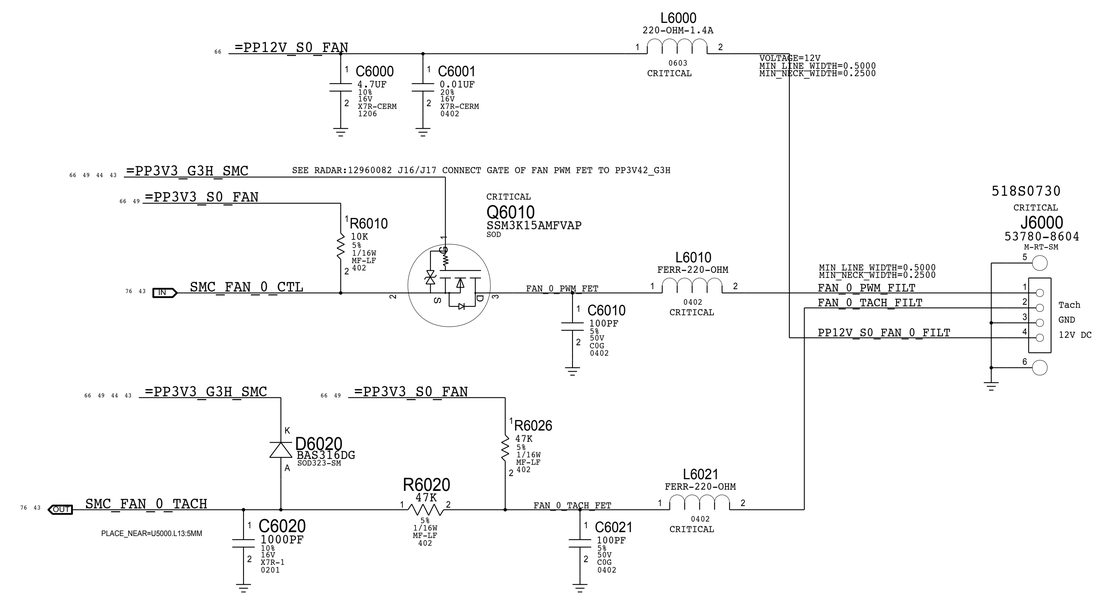
	SHEET: 48 OF 81

SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Protol Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
System Fan

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DRAWING NUMBER 051-00081 SIZE D
REVISION 3.0.0
BRANCH
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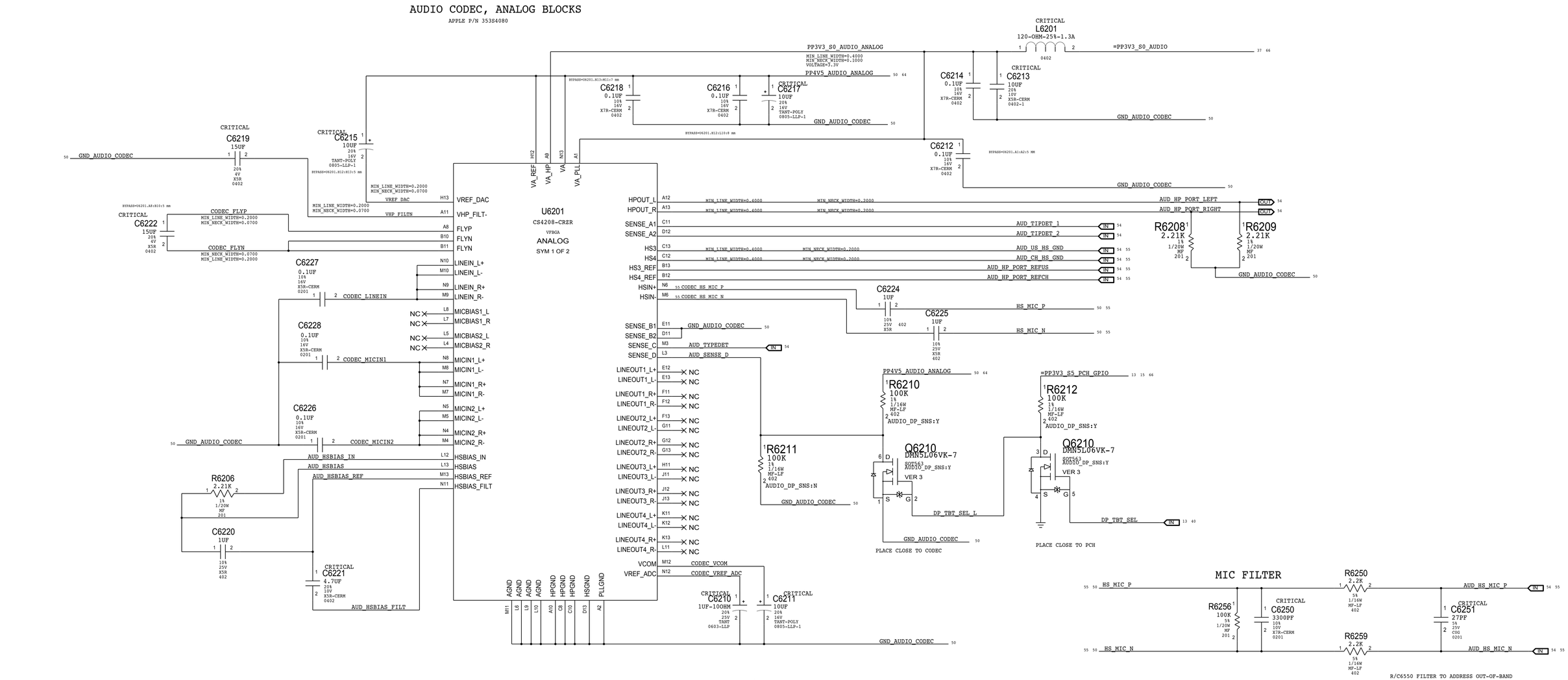
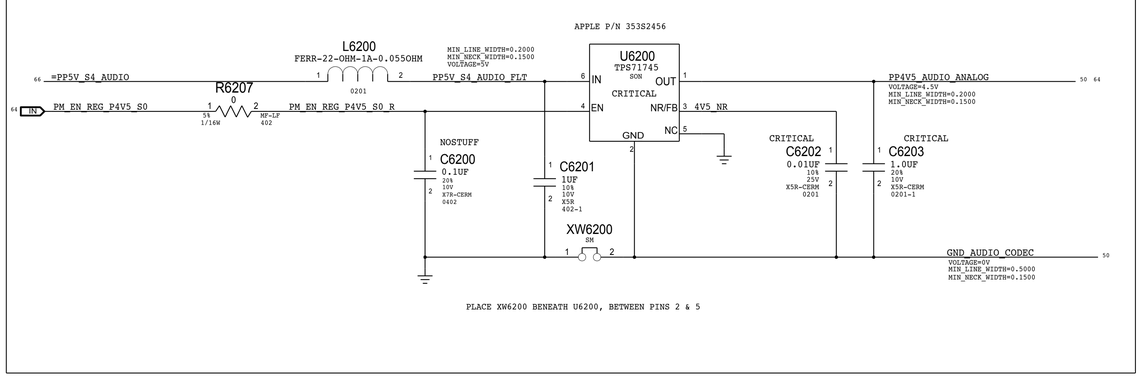
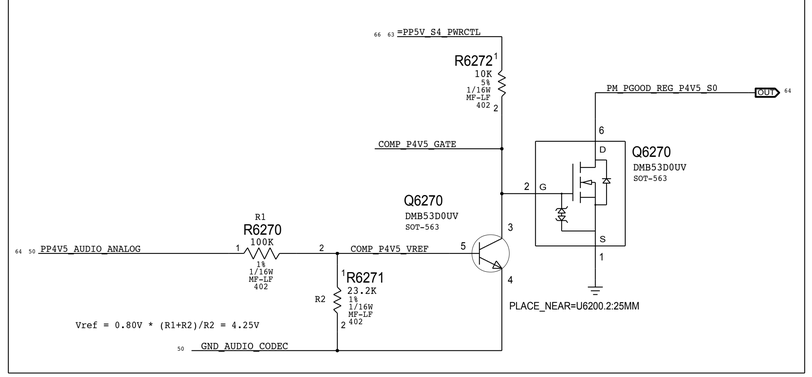


4.5V POWER SUPPLY FOR CODEC



4.5V COMPARATOR



SYNC_MASTER=J117_GAREN	SYNC_DATE=05/05/2014
PAGE TITLE: AUDIO: Codec (Analog)	
Apple Inc.	DRAWING NUMBER: 051-00081 — SIZE: D
	REVISION: 3.0.0
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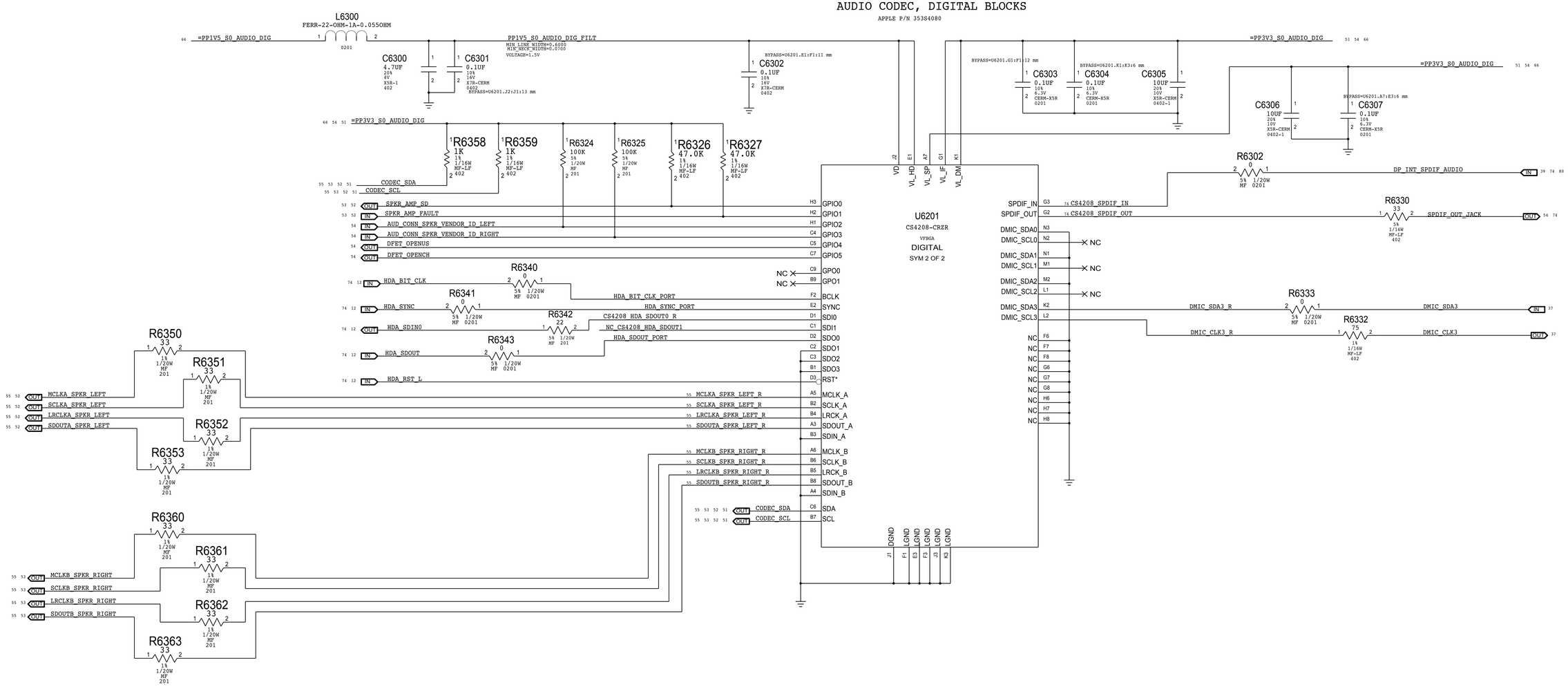
	PAGE: 62 OF 123
	SHEET: 50 OF 81

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=J117_GAREN	SYNC_DATE=05/05/2014
PAGE TITLE	AUDIO:CODEC, DIGITAL
Apple Inc.	DRAWING NUMBER 051-00081 SIZE D
	REVISION 3.0.0
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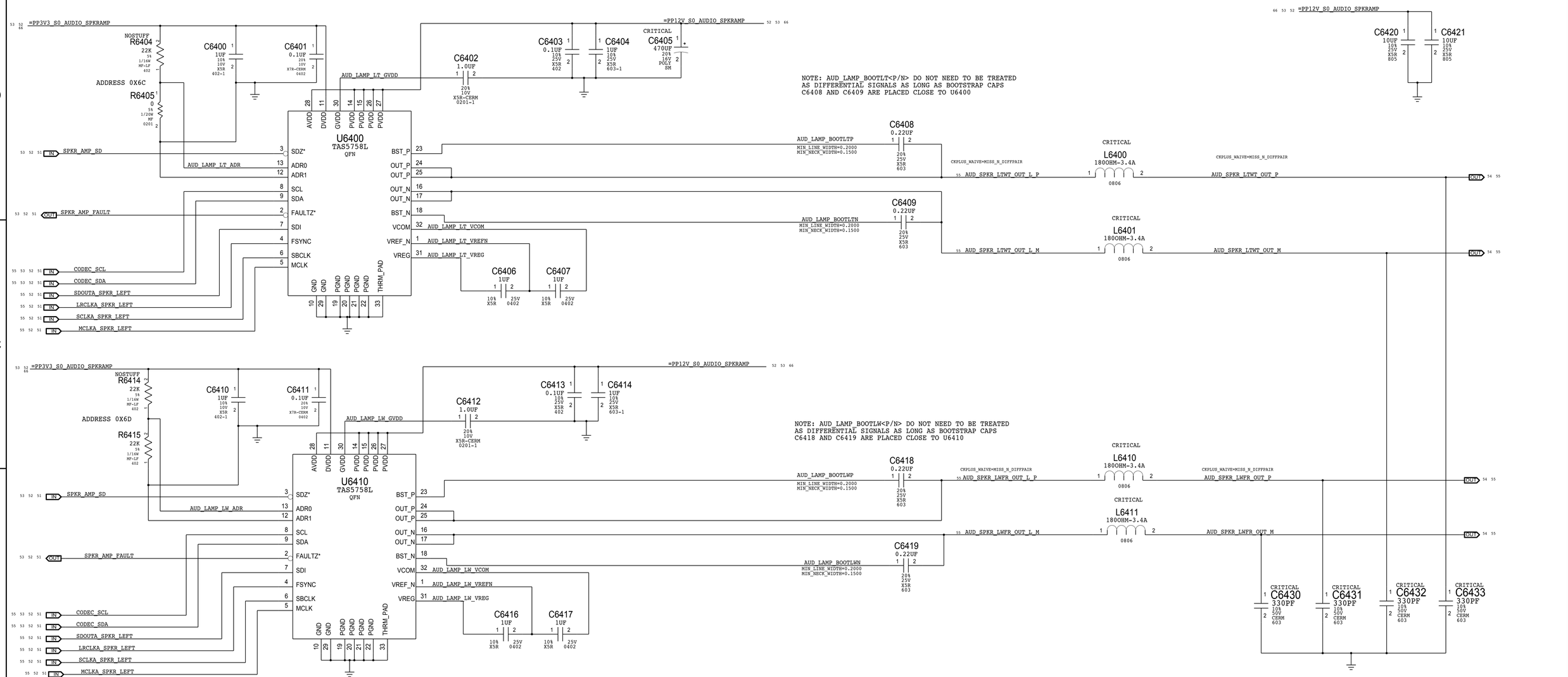
2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD GAIN = TBD

SPEAKER AMPLIFIERS - LEFT CHANNEL



SYNC_MASTER=J117_GAKEN SYNC_DATE=05/05/2014

PAGE TITLE

AUDIO: SPEAKER AMP, LEFT CHANNEL

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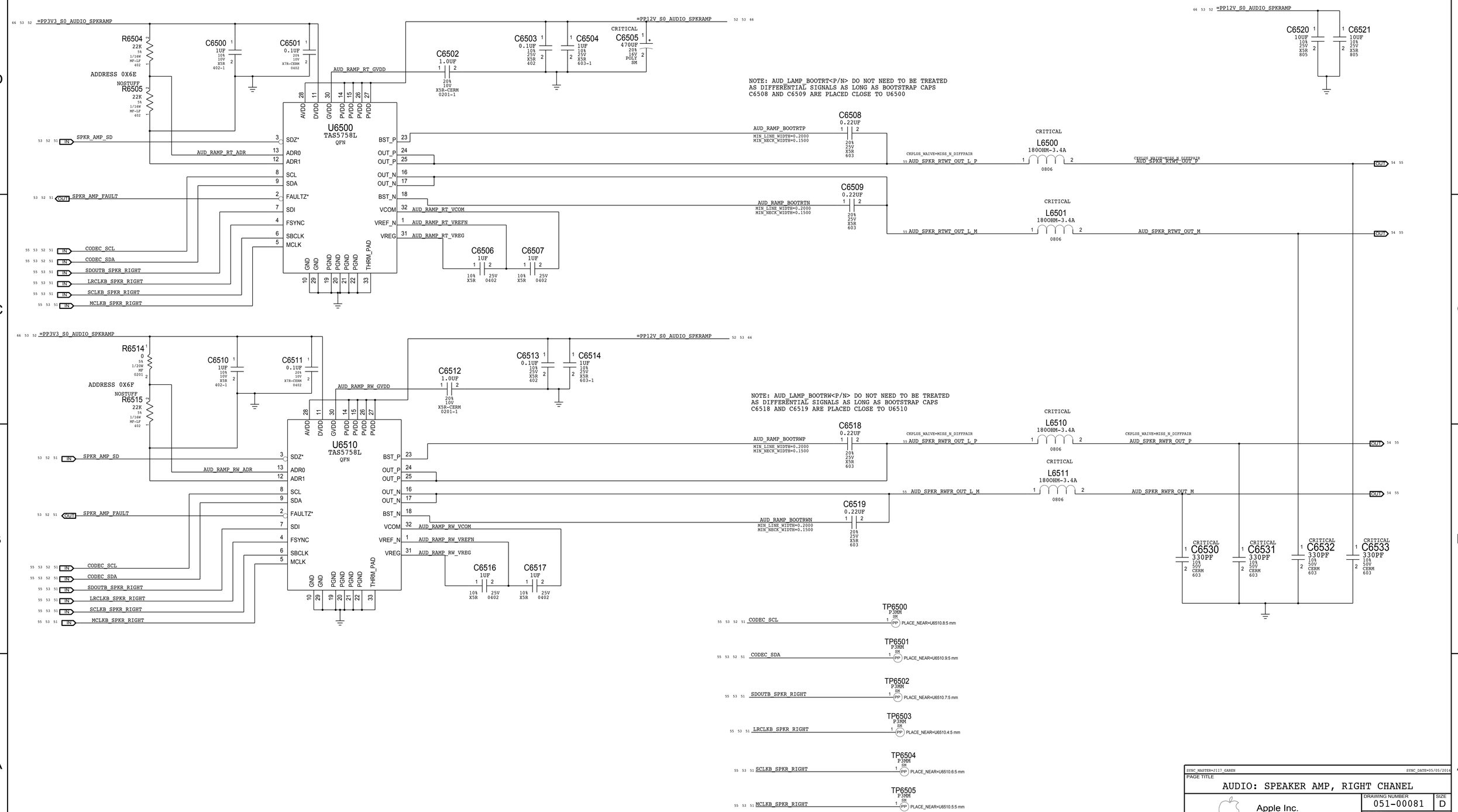
SPEAKER AMPLIFIERS - RIGHT CHANNEL



SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE

AUDIO: SPEAKER AMP, RIGHT CHANEL

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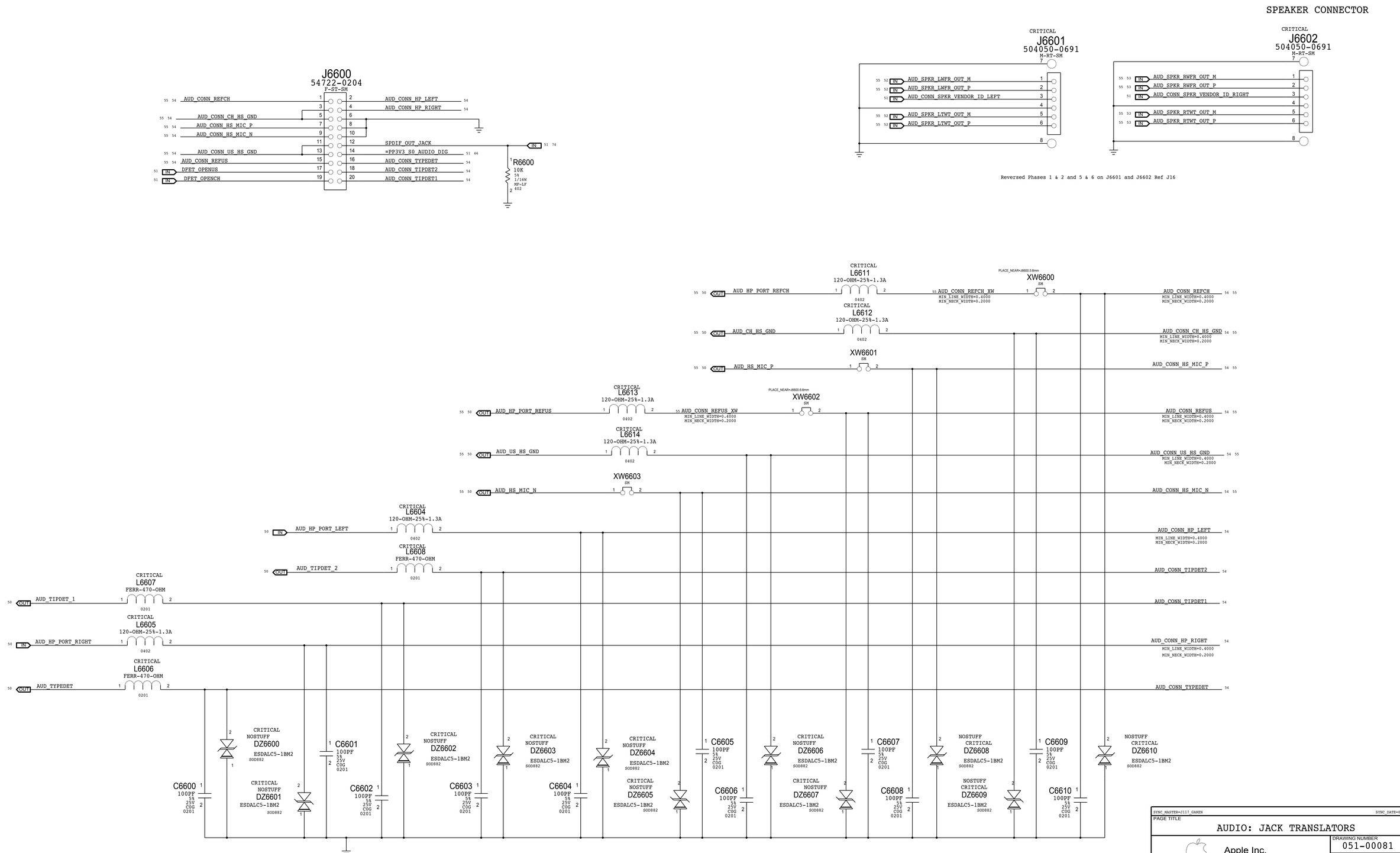
SPEAKER CONNECTOR
J6600
54722-0204
F-ST-SM
AUD_CONN_REFCH
AUD_CONN_HP_LEFT
AUD_CONN_HP_RIGHT
AUD_CONN_CH_HS_GND
AUD_CONN_HS_MIC_P
AUD_CONN_HS_MIC_N
SPDIF_OUT_JACK
AUD_CONN_US_HS_GND
=PP3V3_S0_AUDIO_DIG
AUD_CONN_REFUS
AUD_CONN_TYPEDET
DFET_OPENUS
AUD_CONN_TIPDET2
DFET_OPENCH
AUD_CONN_TIPDET1
R6600
10K
5%
1/16W
MF-LF
402
CRITICAL
J6601
504050-0691
M-RT-SM
AUD_SPKR_LWFR_OUT_M
AUD_SPKR_LWFR_OUT_P
AUD_CONN_SPKR_VENDOR_ID_LEFT
AUD_SPKR_LTWT_OUT_M
AUD_SPKR_LTWT_OUT_P
CRITICAL
J6602
504050-0691
M-RT-SM
AUD_SPKR_RWFR_OUT_M
AUD_SPKR_RWFR_OUT_P
AUD_CONN_SPKR_VENDOR_ID_RIGHT
AUD_SPKR_RTWT_OUT_M
AUD_SPKR_RTWT_OUT_P
Reversed Phases 1 & 2 and 5 & 6 on J6601 and J6602 Ref J16
CRITICAL
L6611
120-OHM-25%-1.3A
0402
AUD_HP_PORT_REFCH
AUD_CONN_REFCH_XW
PLACE_NEAR=J6600:0.8mm
XW6600
SM
AUD_CONN_REFCH
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
CRITICAL
L6612
120-OHM-25%-1.3A
0402
AUD_CH_HS_GND
AUD_CONN_CH_HS_GND
XW6601
SM
AUD_HS_MIC_P
AUD_CONN_HS_MIC_P
CRITICAL
L6613
120-OHM-25%-1.3A
0402
AUD_HP_PORT_REFUS
AUD_CONN_REFUS_XW
PLACE_NEAR=J6600:0.8mm
XW6602
SM
AUD_CONN_REFUS
CRITICAL
L6614
120-OHM-25%-1.3A
0402
AUD_US_HS_GND
AUD_CONN_US_HS_GND
XW6603
SM
AUD_HS_MIC_N
AUD_CONN_HS_MIC_N
CRITICAL
L6604
120-OHM-25%-1.3A
0402
AUD_HP_PORT_LEFT
AUD_CONN_HP_LEFT
CRITICAL
L6608
FERR-470-OHM
0201
AUD_TIPDET_2
AUD_CONN_TIPDET2
CRITICAL
L6607
FERR-470-OHM
0201
AUD_TIPDET_1
AUD_CONN_TIPDET1
CRITICAL
L6605
120-OHM-25%-1.3A
0402
AUD_HP_PORT_RIGHT
AUD_CONN_HP_RIGHT
CRITICAL
L6606
FERR-470-OHM
0201
AUD_TYPEDET
AUD_CONN_TYPEDET
C6600
100PF
5%
25V
C0G
0201
CRITICAL
NOSTUFF
DZ6600
ESDALC5-1BM2
SOD882
CRITICAL
NOSTUFF
DZ6601
ESDALC5-1BM2
SOD882
C6601
100PF
5%
25V
C0G
0201
C6602
100PF
5%
25V
C0G
0201
CRITICAL
NOSTUFF
DZ6602
ESDALC5-1BM2
SOD882
C6603
100PF
5%
25V
C0G
0201
CRITICAL
NOSTUFF
DZ6603
ESDALC5-1BM2
SOD882
C6604
100PF
5%
25V
C0G
0201
CRITICAL
NOSTUFF
DZ6604
ESDALC5-1BM2
SOD882
CRITICAL
NOSTUFF
DZ6605
ESDALC5-1BM2
SOD882
C6605
100PF
5%
25V
C0G
0201
C6606
100PF
5%
25V
C0G
0201
CRITICAL
NOSTUFF
DZ6606
ESDALC5-1BM2
SOD882
CRITICAL
NOSTUFF
DZ6607
ESDALC5-1BM2
SOD882
C6607
100PF
5%
25V
C0G
0201
C6608
100PF
5%
25V
C0G
0201
NOSTUFF
CRITICAL
DZ6608
ESDALC5-1BM2
SOD882
NOSTUFF
CRITICAL
DZ6609
ESDALC5-1BM2
SOD882
C6609
100PF
5%
25V
C0G
0201
C6610
100PF
5%
25V
C0G
0201
NOSTUFF
CRITICAL
DZ6610
ESDALC5-1BM2
SOD882
ESD DIODES (DZ6600 -> DZ6610) NOW NOSTUFF - MAY BE ADDED FOLLOWING ESD TESTING
SYNC_MASTER=J117_GAREN
SYNC_DATE=05/05/2014
PAGE TITLE
AUDIO: JACK TRANSLATORS
Apple Inc.
DRAWING NUMBER
051-00081
SIZE
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REVISION
3.0.0
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR_INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	0.1 MM	?
SPKROUT_ISO	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
AUDIODIFF_2MM	*	Y	0.2 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
SPKROUT	*	*	SPKROUT_ISO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SPEAKER OUTPUTS				
I205 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	53 54
I203 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_M	53 54
I220	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_P	53
I219	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_M	53
I333 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	53 54
I332 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_M	53 54
I330	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_P	53
I331	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_M	53
I337 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	52 54
I336 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_M	52 54
I334	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_P	52
I335	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_M	52
I341 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	52 54
I340 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_M	52 54
I338	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_P	52
I339	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_M	52
HEADSET MIC				
I348 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_P	54
I349 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_N	54
I254 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	50 54
I255 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	50 54
I324 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_P	50
I325 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_N	50
I343 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_P	50
I342 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_N	50
I353		AUDIO	AUD_CONN_CH_HS_GND	54
I355		AUDIO	AUD_CONN_US_HS_GND	54
I368		AUDIO	AUD_CH_HS_GND	50 54
I369		AUDIO	AUD_US_HS_GND	50 54
I356		AUDIO	AUD_CONN_REFCH	54
I357		AUDIO	AUD_CONN_REFUS	54
I371		AUDIO	AUD_CONN_REFCH_XW	54
I370		AUDIO	AUD_CONN_REFUS_XW	54
I373		AUDIO	AUD_HP_PORT_REFCH	50 54
I372		AUDIO	AUD_HP_PORT_REFUS	50 54

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CODEC SCL & SDA				
I358			CODEC_SCL	51 52 53
I359			CODEC_SDA	51 52 53
TDM				
I360		HSA	MCLKA_SPKR_LEFT	51 52
I361		HSA	SCLKA_SPKR_LEFT	51 52
I362		HSA	LRCLKA_SPKR_LEFT	51 52
I363		HSA	SDOUTA_SPKR_LEFT	51 52
I374			MCLKA_SPKR_LEFT_R	51
I375			SCLKA_SPKR_LEFT_R	51
I376			LRCLKA_SPKR_LEFT_R	51
I377			SDOUTA_SPKR_LEFT_R	51
I364		HSA	MCLKB_SPKR_RIGHT	51 53
I365		HSA	SCLKB_SPKR_RIGHT	51 53
I367		HSA	LRCLKB_SPKR_RIGHT	51 53
I366		HSA	SDOUTB_SPKR_RIGHT	51 53
I379			MCLKB_SPKR_RIGHT_R	51
I378			SCLKB_SPKR_RIGHT_R	51
I380			LRCLKB_SPKR_RIGHT_R	51
I381			SDOUTB_SPKR_RIGHT_R	51

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

AUDIO: Speaker ID

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DRAWING NUMBER 051-00081 SIZE D

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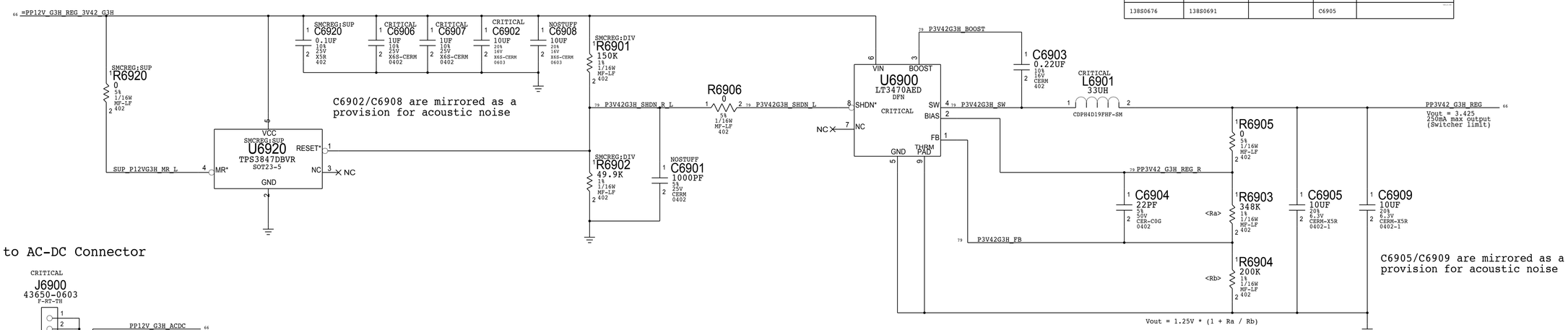
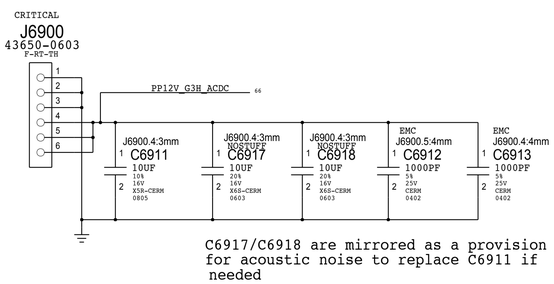
3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

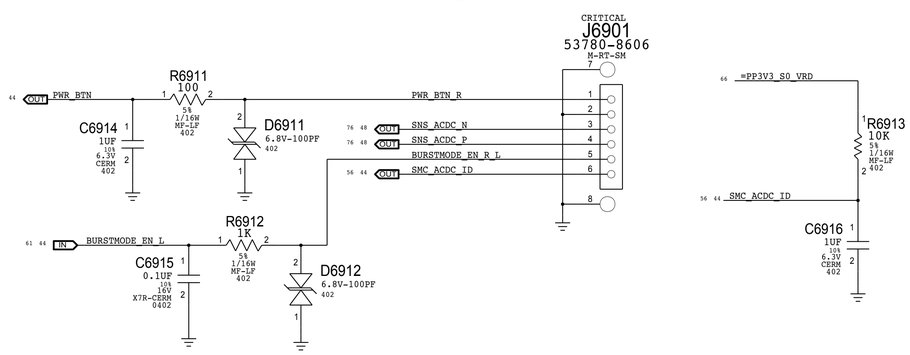
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	



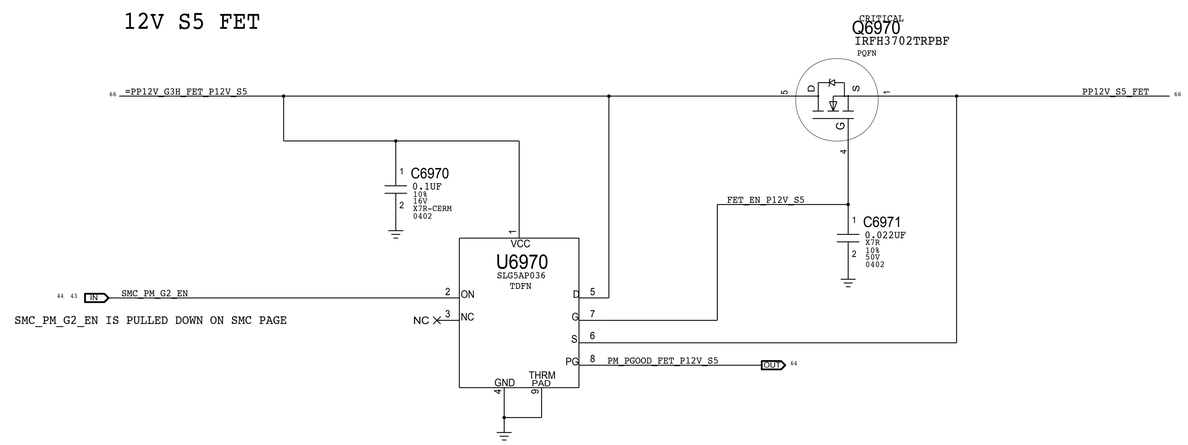
MLB to AC-DC Connector



MLB to AC-DC Supplemental Signal Connector



12V S5 FET



SYNC_MASTER=J117 ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: Power Connectors / VReg G3Hot

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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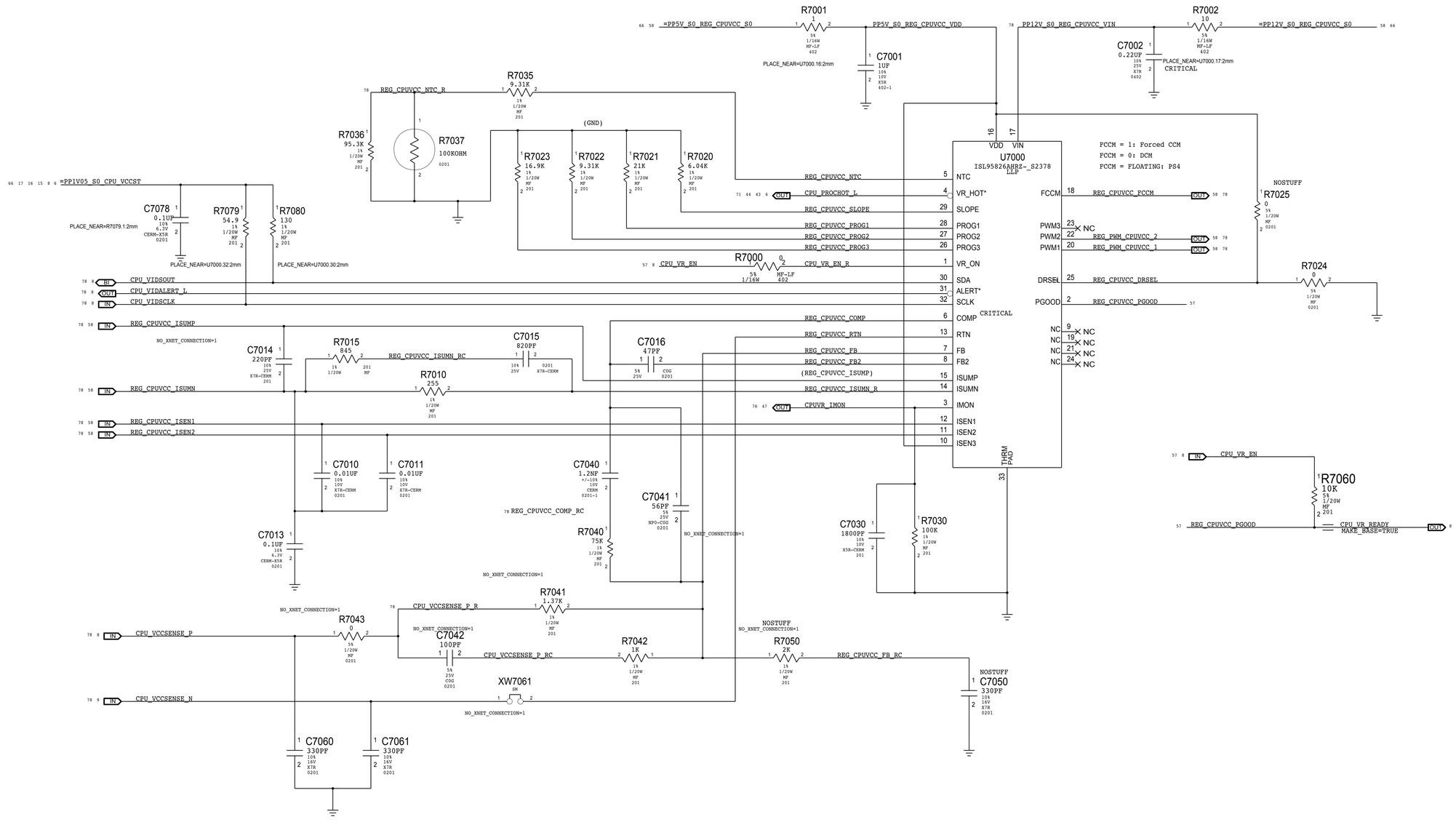

SYNC_MASTER=J70_ROSSANA SYNC_DATE=09/17/2013

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-00081

SIZE D

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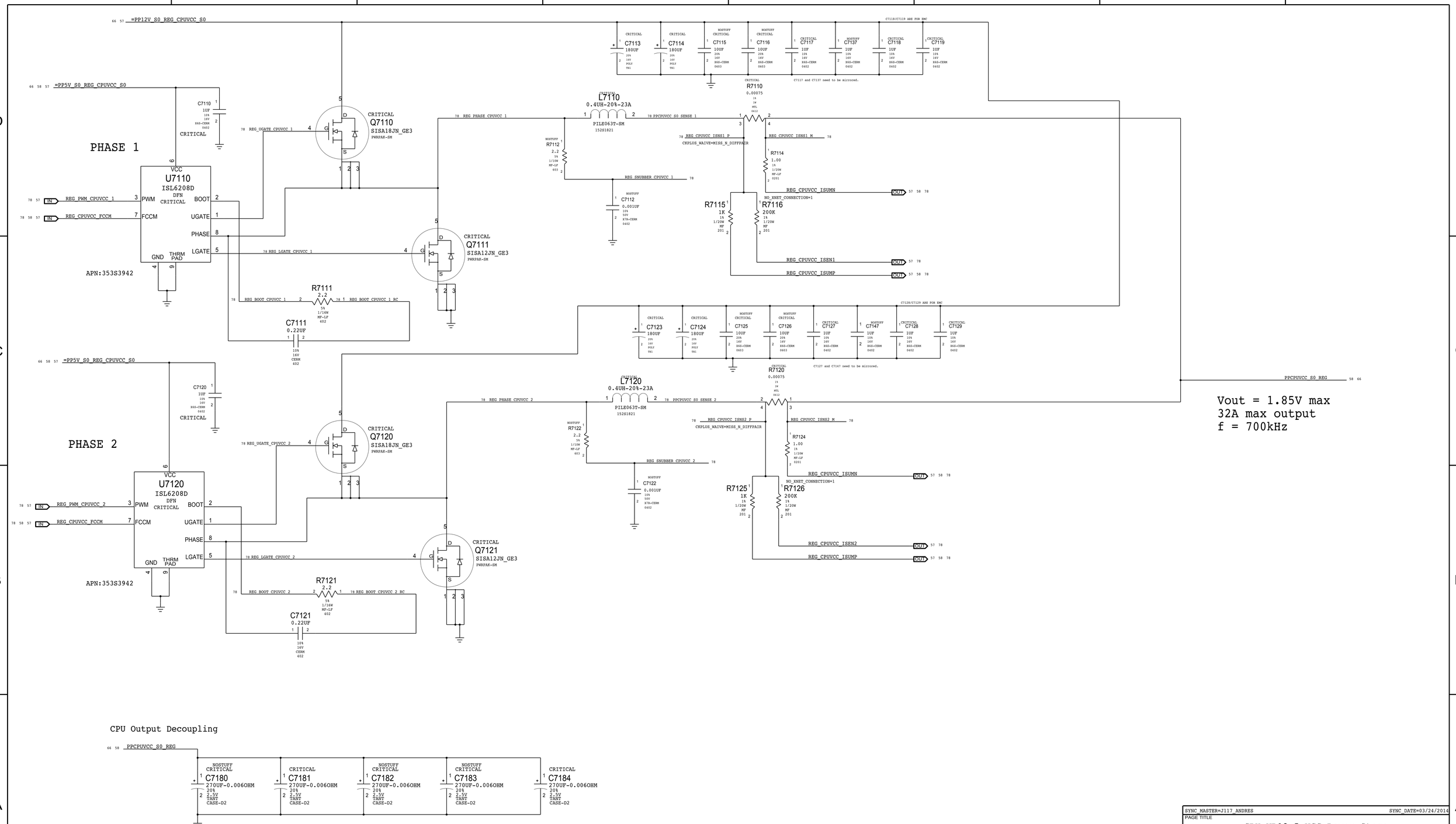

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

CPU VR12.5 VCC Power Stage

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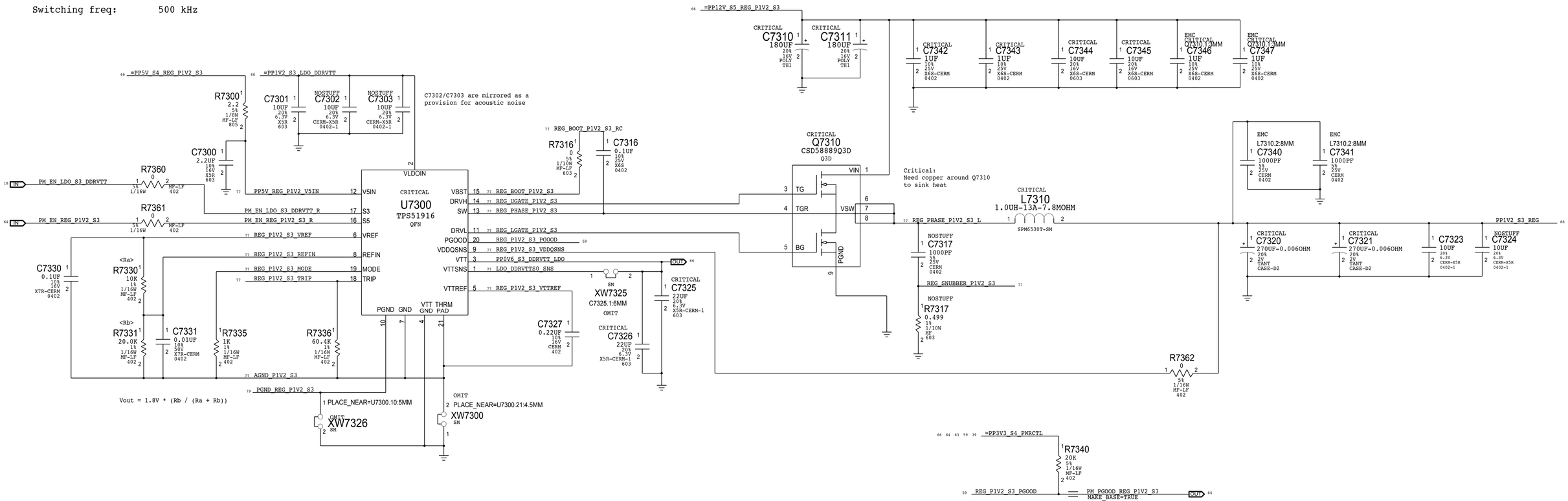
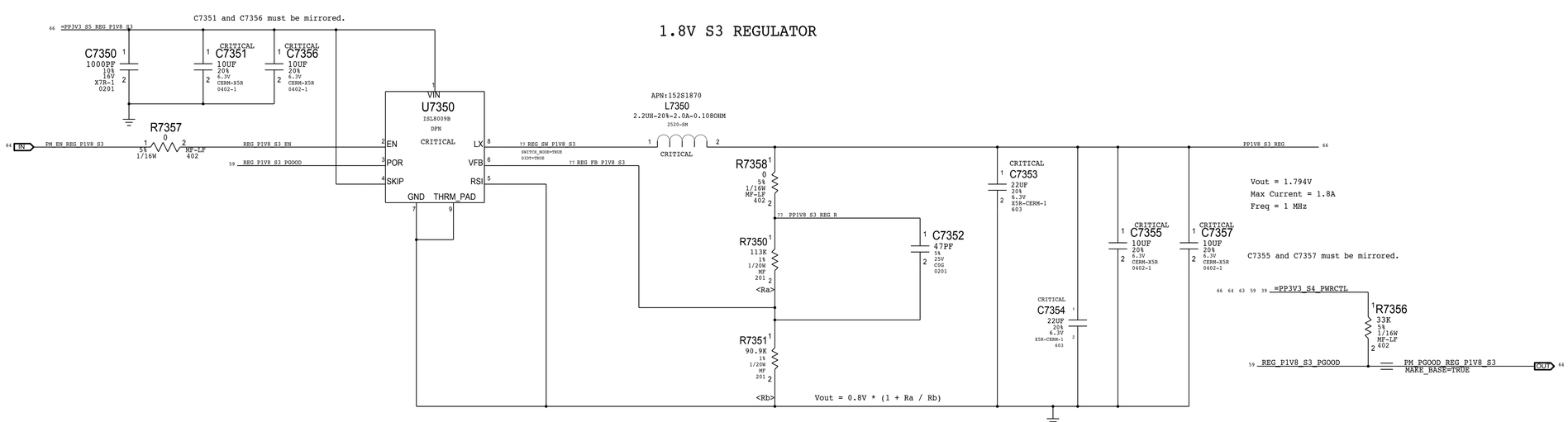
VDDQ 1.2V S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5 * Rds(Q7310)} + \frac{0.65625}{L7310 * f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz





SYNC MASTER=J70 ROSSANA SYNC DATE=09/12/2013

PAGE TITLE
VReg VDDQ S3 / 1.8V S3

Apple Inc.

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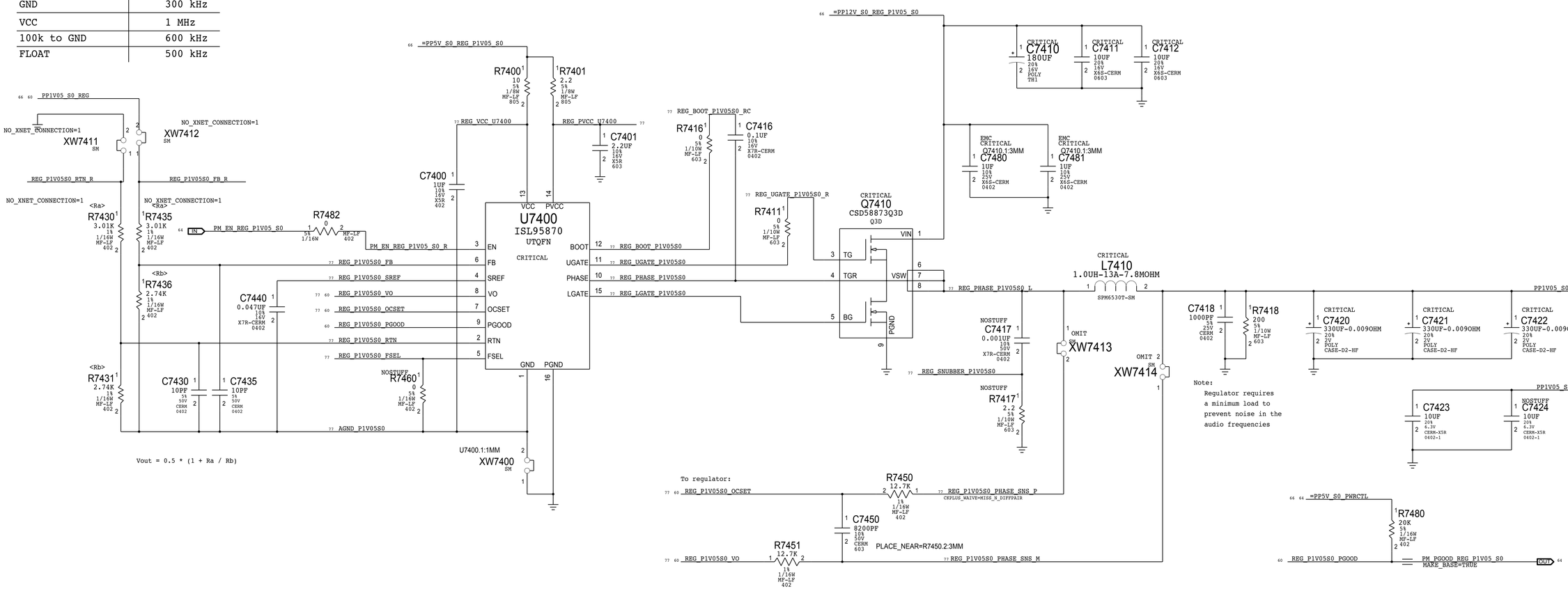
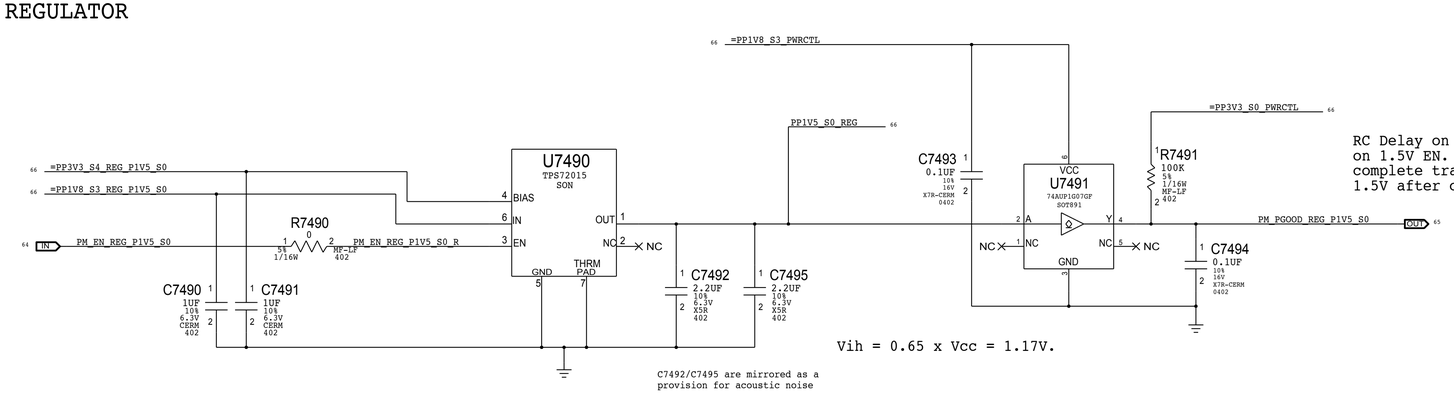
PCH (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{R7450 * 8.5\ E\text{-}6}{DCR(L7410)}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



1.5V S0 REGULATOR



RC Delay on 1.5V PGOOD must be longer than delay on 1.5V EN. This allows for rail voltage to complete transition from Vih min (1.17V) to 1.5V after output shifts to OD.

SYNC MASTER=J117 ANDRES SYNC DATE=03/24/2014

PAGE TITLE: VREG 1V05 S0 / 1V5 S0

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3.3V S5 Regulator

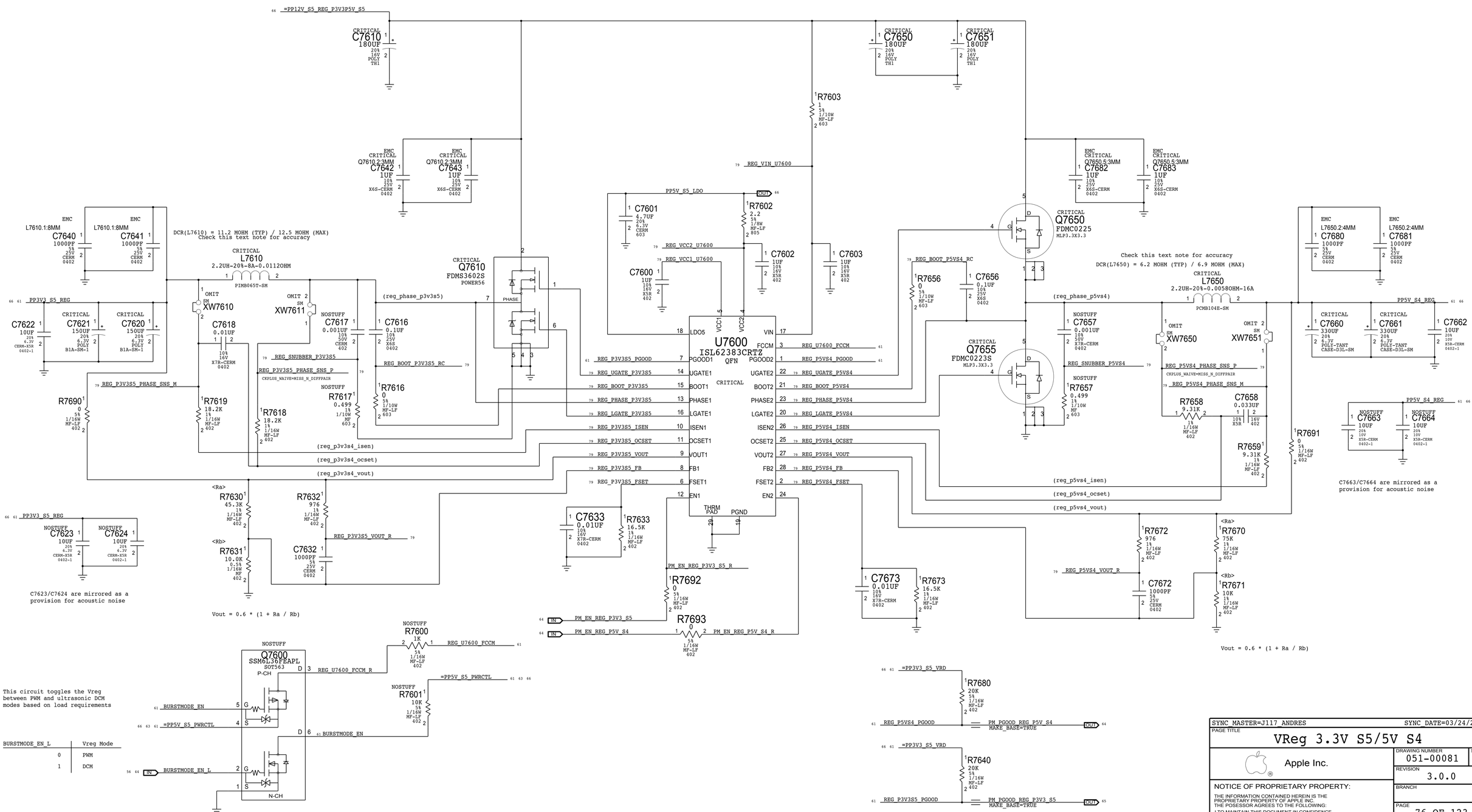
OC trip point: 12.5 A = $\frac{R7618 * 10 E-6}{DCR(L7610)}$

Switching freq: 356 kHz = $\frac{1}{170 E-12 * R7633}$

5V S4 Regulator

OC trip point: 14.1 A = $\frac{R7658 * 10 E-6}{DCR(L7650)}$

Switching freq: 356 kHz = $\frac{1}{170 E-12 * R7673}$



This circuit toggles the Vreg between PWM and ultrasonic DCM modes based on load requirements

BURSTMODE_EN_L	Vreg Mode
0	PWM
1	DCM

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: VReg 3.3V S5/5V S4

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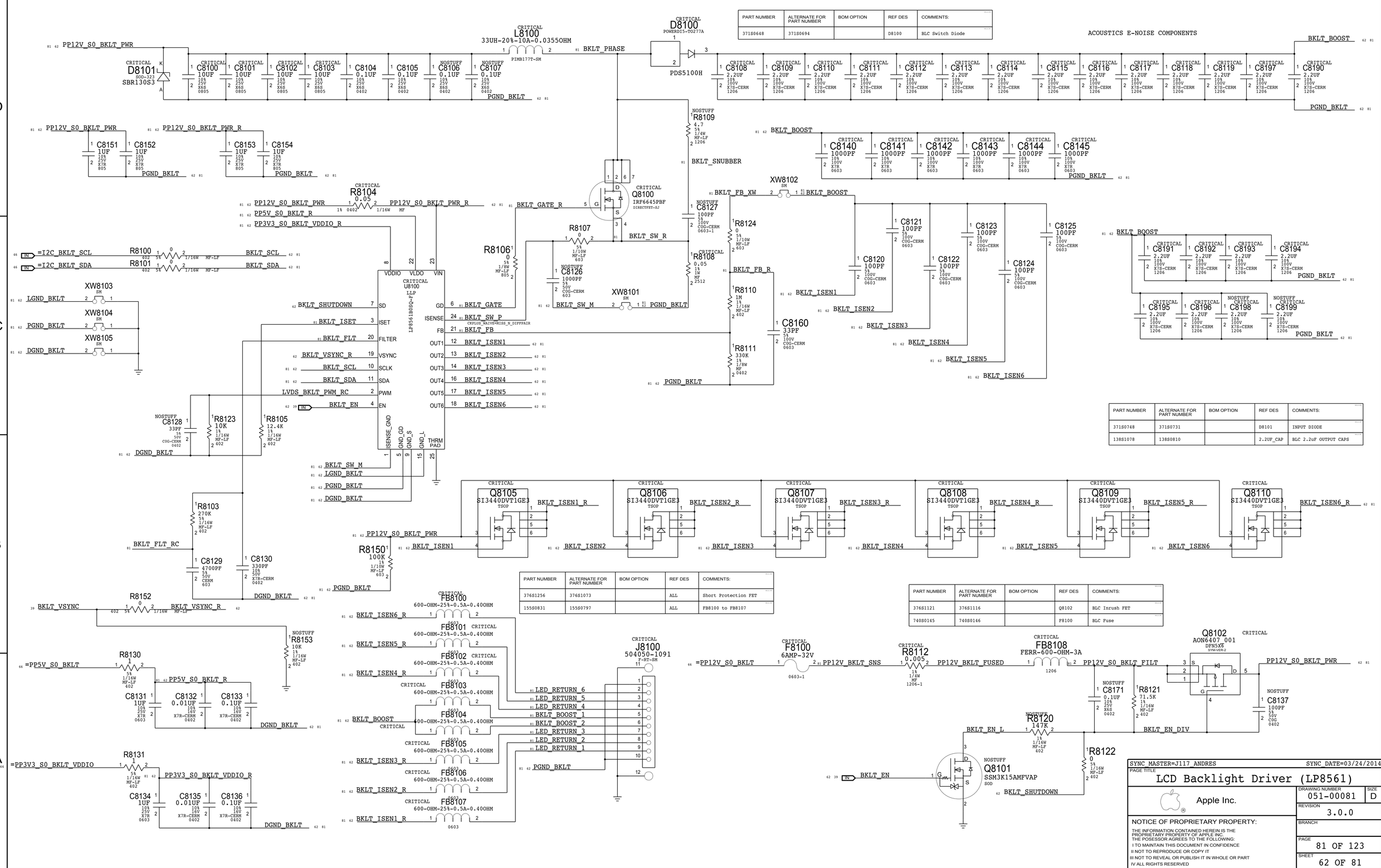
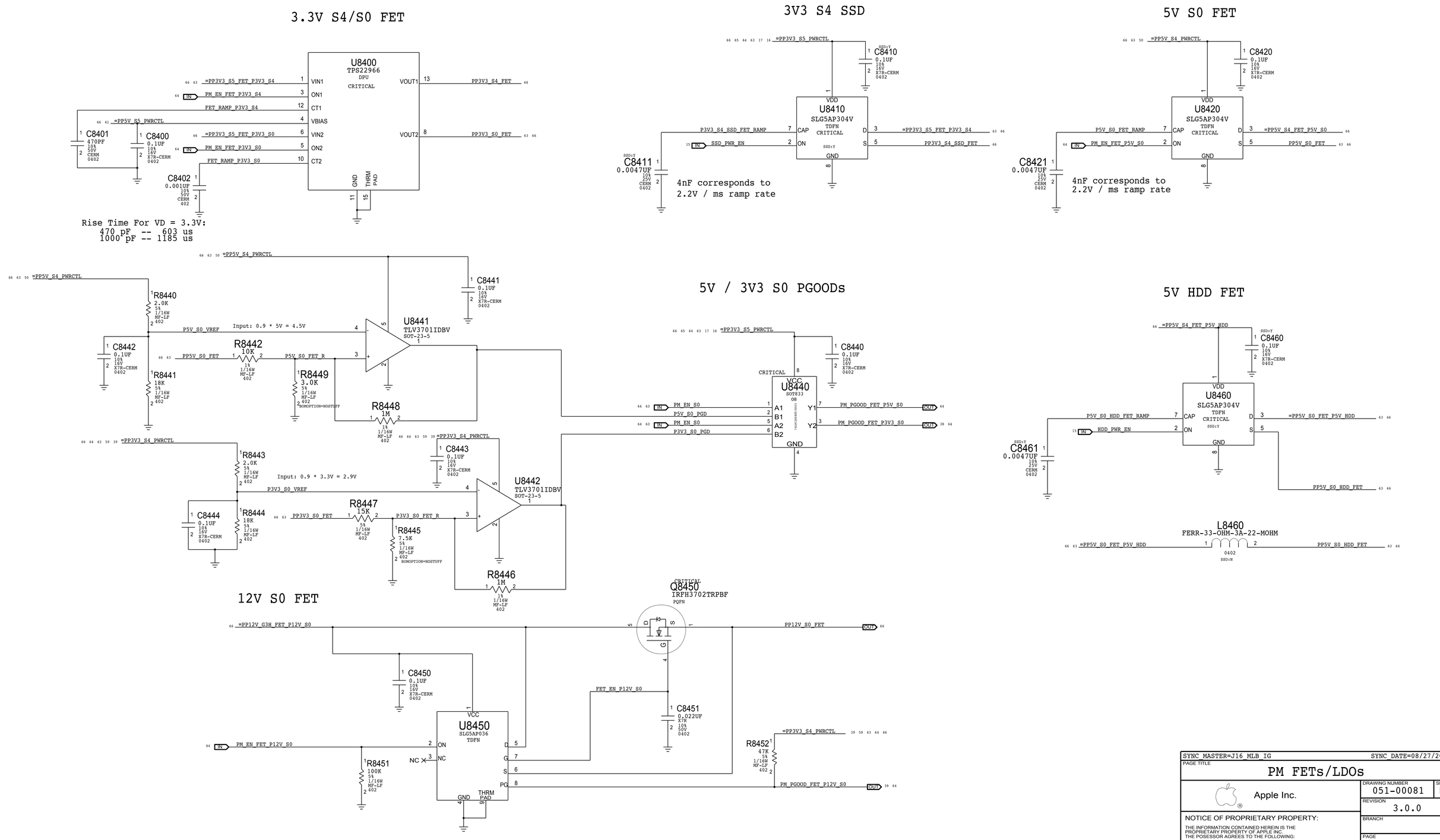


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0648	371S0694		D8100	BLC Switch Diode

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0748	371S0731		D8101	INPUT DIODE
138S1078	138S0810		2.2UF_CAP	BLC 2.2uF OUTPUT CAPS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
PM FETs/LDOs

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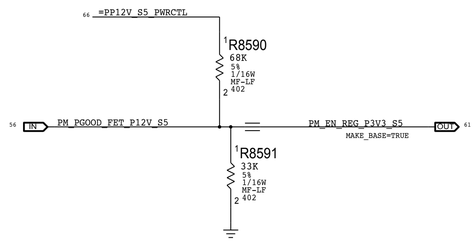
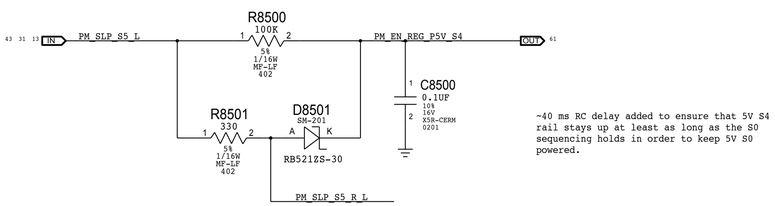
S5 Enables

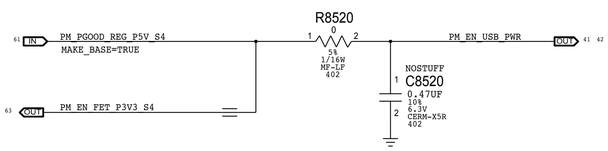


S4 Enables

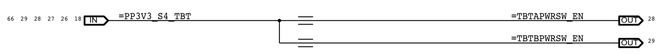


~40 ms RC delay added to ensure that 5V S4 rail stays up at least as long as the S0 sequencing holds in order to keep 5V S0 powered.

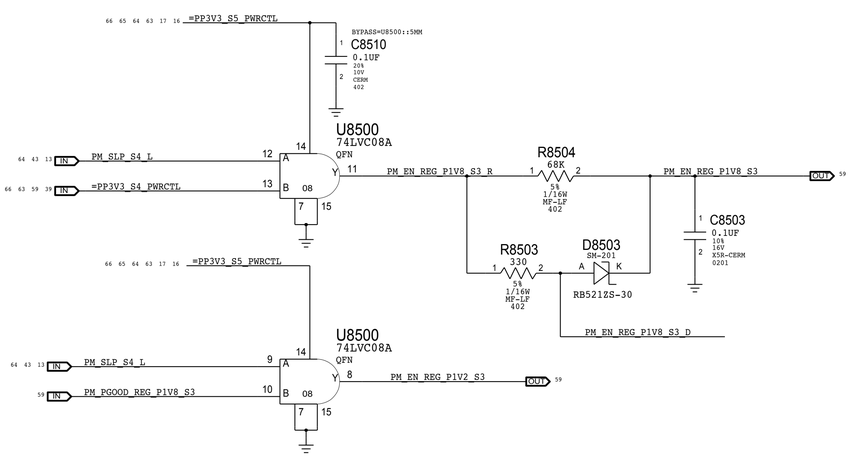
S4 USB Enable



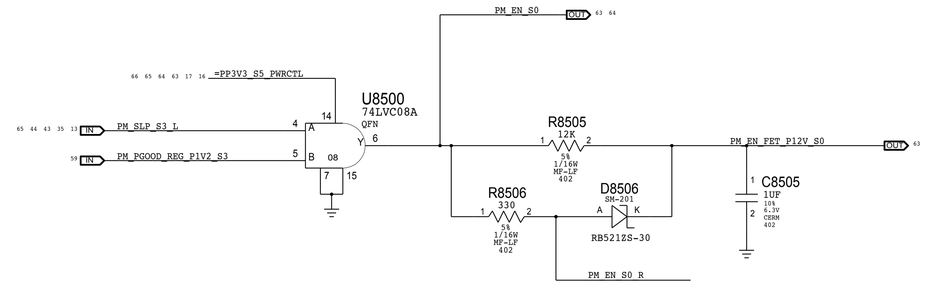
S4 TBT Port Enable



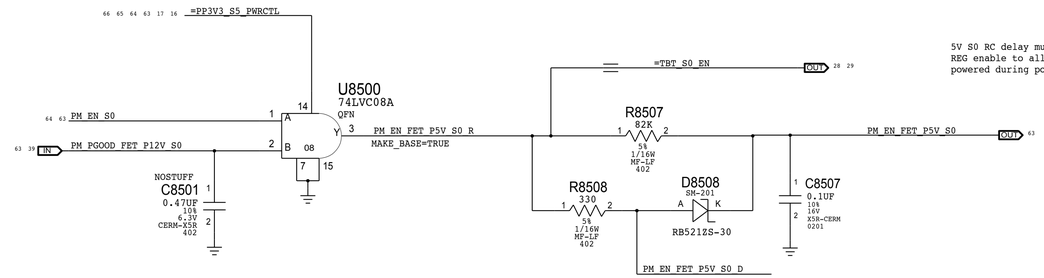
S3 Enables



S0 Enables

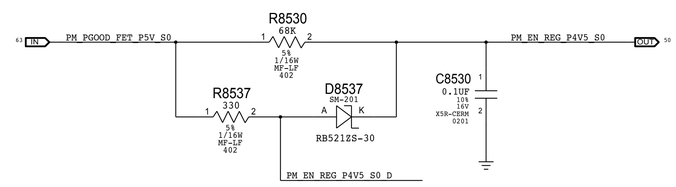


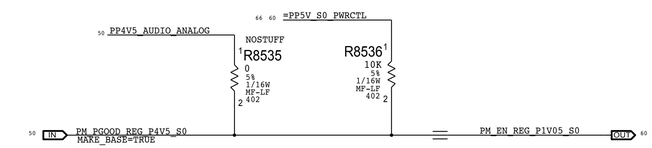
12V S0 EN RC delay must be >= downstream delay on 4.5V REG enable which in turn enables 1.05V S0. This allows for 12V S0 to hold as long as 1.05V S0 regulator is powered.



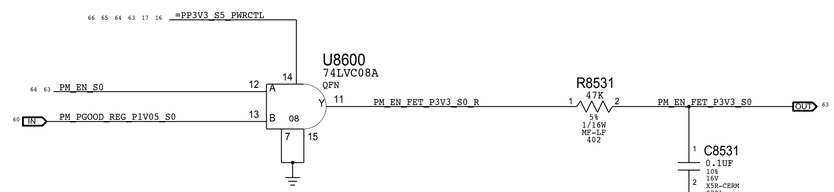
5V S0 RC delay must be >= downstream delay on 4.5V REG enable to allow for 4.5V regulator to remain powered during power down sequence.

Audio + PCH Sequencing Requirements:
4.5V -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD

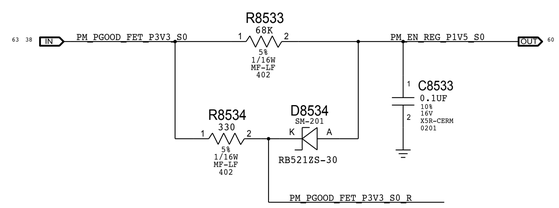




NOSTUFF resistor added in case of using 4.5V rail as the PGOOD itself directly.



No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 5V S0 on 1.05V VR page competing with logic turn on time.



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PAGE TITLE
PM Regulator Enables

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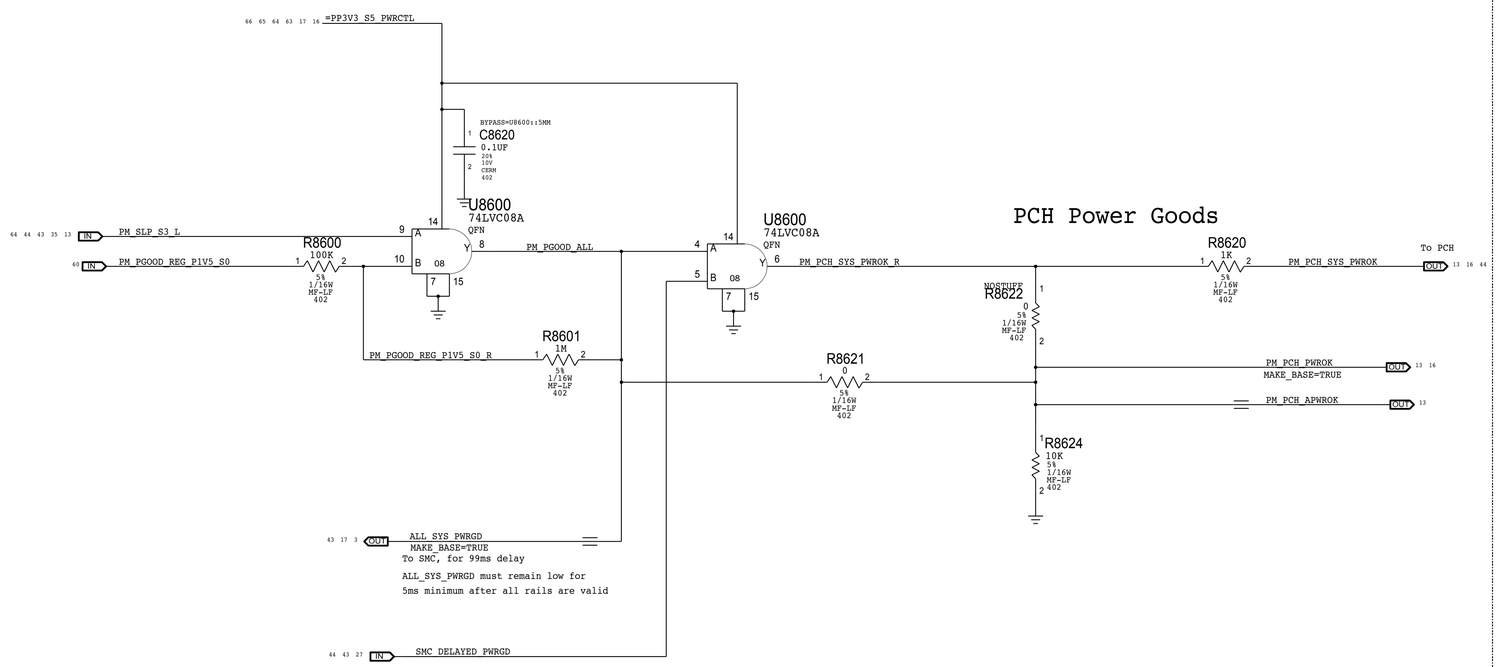
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



Resume Reset

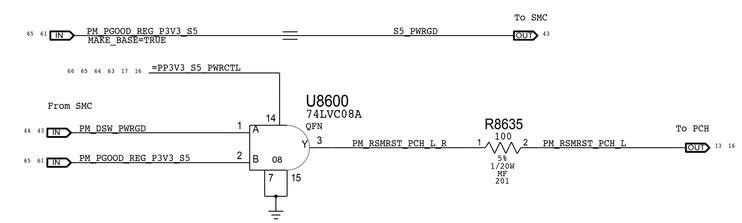
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 1.8V and 1.2V for DDR3

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

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PM Power Good

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G3 Rails

Always on: Keeps the PCH RTC alive

79	PP3V3_G3 MAKE_BASE=TRUE	PP3V3_G3_RTC	17
		=PPVRTC_G3_PCH	8 12 13

G3H Rails

79	PP12V_ACDC MAKE_BASE=TRUE	PP12V_G3H_ACDC	56
		=PP12V_G3H_SNS_R	47
79	PP12V_G3H MAKE_BASE=TRUE	PP12V_G3H_SNS	47
		=PP12V_G3H_REG_3V42_G3H	56
		=PP12V_G3H_FET_P12V_S5	56
		=PP12V_G3H_FET_P12V_S0	63
79	PP3V42_G3H MAKE_BASE=TRUE	PP3V42_G3H_REG	56
		=PP3V3_G3H_BT	31
		=PP3V3_G3H_SMC	43 44 49
		=PP3V3_G3H_RTC_D	17
		=PPVIN_G3H_SMCVREF	44
		=PP3V3_G3H_SMC_USBMUX	41
		=PP3V3_G3H_T112	45

Ground/Common

GND\G MAKE_BASE=TRUE	

S5 Rails

Enabled when system has AC and is in S5

79	PP12V_S5 MAKE_BASE=TRUE	PP12V_S5_FET	56
		=PP12V_S5_REG_P3V3P5V_S5	61
		=PP12V_S5_REG_P1V2_S3	59
		=PPHV_SW_TBTAPWRSW	28
		=PPHV_SW_TBTBPWRSW	29
		=PP12V_S5_SNS	47
		=PP12V_S5_PWRCTL	64
79	PP5V_S5 MAKE_BASE=TRUE	I2326 PP5V_S5_LDO	61
		NBC =PP5V_S5_PWRCTL	61 63
79	PP3V3_S5 MAKE_BASE=TRUE	PP3V3_S5_REG	61
		=PP3V3_S5_FET_P3V3_S4	63
		=PP3V3_S5_FET_P3V3_S0	63
		=PP3V3_S5_PWRCTL	16 17 63 64 65
		=PP3V3_S5_VRD	61
		=PP3V3_S5_LED	3
		=PP3V3_SUS_PCH_VCCSUS_GPIO	8 11
		=PP3V3_S5_PCH_VCCDSW	8 11
		=PP3V3_SUS_PCH_VCC_SPI	8 11 14
		=PP3V3_SUS_PCH_VCCSUS_RTC	8 11
		=PP3V3_SUS_PCH_VCCSUS_ICC	8
		=PP3V3_S5_ROM	45
		=PP3V3_S5_SENSE	47
		=PP3V3_S5_SMC	44
		=PP3V3_S4_TBTAPWRSW	28
		=PP3V3_S4_TBTBPWRSW	29
		=PP3V3_SUS_PCH_GPIO	14
		=PP3V3_S5_PCH_GPIO	13 15 50
		=PP3V3_S5_REG_P1V8_S3	59
		=PP3V3_S5_XDP	16

S4 Rails

Enabled when system has AC and is in run or sleep

79	PP5V_S4 MAKE_BASE=TRUE	PP5V_S4_REG	61
		=PP5V_S4_REG_P1V2_S3	59
		=PP5V_S4_FET_P5V_S0	63
		=PP5V_S4_PWRCTL	50 63
		=PP5V_S4_USB	41 42
		=PP5V_S4_AUDIO	50
		=PP5V_S4_FET_P5V_HDD	63
		=PP5V_S4_SDCARD	36
79	PP3V3_S4 MAKE_BASE=TRUE	PP3V3_S4_FET	63
		=PP3V3_S4_FET_ENET	35
		=PP3V3_S4_PWRCTL	39 59 63 64
		=PP3V3_S4_LED	3
		=PP3V3_S4_PCH_GPIO	15 18 41 42
		=PP3V3_S4_SDCARD	36
		=PP3V3_S4_SMC	44
		=PP3V3_S4_TBT	18 26 27 28 29 64
		=PP3V3_S4_AP	31 44
		=PP3V3_S4_REG_P1V5_S0	60

S3 Rails

Enabled when system is in run or sleep

79	PP3V3_ENET MAKE_BASE=TRUE	PP3V3_ENET_FET	35
		=PP3V3_ENET_PHY	34 35
77	PP1V8_S3 MAKE_BASE=TRUE	PP1V8_S3_REG	59
		=PP1V8_S3_DDR	21 22 23 24
		=PP1V8_S3_CAMERA_FET	38
		=PP1V8_S3_PWRCTL	60
		=PP1V8_S3_REG_P1V5_S0	60
77	PP1V2_S3 MAKE_BASE=TRUE	PP1V2_S3_REG	59
		=PP1V2_S3_SNS_DDR_R	47
77	PP1V2_S3_DDR MAKE_BASE=TRUE	PP1V2_S3_SNS_DDR	47
		=PP1V2_S3_LDO_DDRVTT	59
		=PP1V2_S3_DDR_MEMVREF	20
		=PP1V2_S3_DDR_VDD2	21 22 23 24
		=PP1V2_S3_DDR_VDDCA	21 22 23 24
		=PP1V2_S3_DDR_VDDQ	21 22 23 24
		=PP1V2_S3_MEM_VTTPWRCTL	18
		=PPVMEMIO_S0_CPU	8 10
		=PP1V2_S3_CAMERA_FET	38
77	PP0V6_S3_DDRVTT MAKE_BASE=TRUE	PP0V6_S3_DDRVTT_LDO	59
		=PP0V6_S3_DDRVTT_A	25
		=PP0V6_S3_DDRVTT_B	25

S0 Rails

Enabled when system is in run

79	PP12V_S0 MAKE_BASE=TRUE	PP12V_S0_FET	63
		=PP12V_S0_REG_CPUVCC_S0	57 58
		=PP12V_S0_REG_P1V05_S0	60
		=PP12V_S0_AUDIO_SPKRAMP	52 53
		=PP12V_S0_BKLT	62
		=PP12V_S0_FAN	49
		=PP12V_S0_LCD	39
79	PP5V_S0 MAKE_BASE=TRUE	PP5V_S0_FET	63
		=PP5V_S0_REG_CPUVCC_S0	57 58
		=PP5V_S0_REG_P1V05_S0	60
		=PP5V_S0_BKLT	62
		=PP5V_S0_FET_P5V_HDD	63
		=PP5V_S0_CAMERA	37 38
		=PP5V_S0_PCH_STRAP	17
		=PP5V_S0_PWRCTL	60 64
79	PP5V_S0_HDD MAKE_BASE=TRUE	PP5V_S0_HDD_FET	63
		=PP5V_S0_SATA	33
79	PP3V3_S0 MAKE_BASE=TRUE	PP3V3_S0_FET	63
		=PP3V3_S0_VRD	56
		=PP3V3_S0_AUDIO	37 50
		=PP3V3_S0_AUDIO_DIG	51 54
		=PP3V3_S0_AUDIO_SPKRAMP	52 53
		=PP3V3_S0_DP	30 39
		=PP3V3_S0_ENET	34
		=PP3V3_S0_FAN	49
		=PP3V3_S0_INTDPMUX	40
		=PP3V3_S0_LED	3
		=PP3V3_S0_PCH	17
		=PP3V3_S0_PCH_VCC3_3_GPIO	8 11
		=PP3V3_S0_PCH_VCCTS	8 11
		=PP3V3_S0_PCH_VCCSDIO	8 11
		=PP3V3_S0_CAMPWREN	
		=PP3V3_S0_SDCARD	36
		=PP3V3_S0_SENSE	32 33 47 48
		=PP3V3_S0_SMBUS	46
		=PP3V3_S0_SMBUS_SMC_0	46
		=PP3V3_S0_SMBUS_SMC_1	39 46
		=PP3V3_S0_SMBUS_SMC_2	46
		=PP3V3_S0_SMBUS_SMC_3	46
		=PP3V3_S0_SMC	44
		=PP3V3_S0_BKLT_VDDIO	62
		=PP3V3_S0_PCH_GPIO	12 13 15 16 27
		=PP3V3_S0_CAMERA	37 38
		=PP3V3_S0_ALS	37
		=PP3V3_S0_MEM_VTTPWRCTL	18
		=PP3V3_S0_PWRCTL	60
79	PP3V3_S4_SSD MAKE_BASE=TRUE	PP3V3_S4_SSD_FET	63
		=PPSSD_S4_SNS_R	47
79	PPSSD_S4 MAKE_BASE=TRUE	PPSSD_S4_SNS	47
		=PPSSD_S4_CONN	32
79	PP1V5_S0 MAKE_BASE=TRUE	PP1V5_S0_REG	60
		=PP1V5_S0_SENSE	33
		=PP1V5_S0_PCH_VCCTS	8
		=PP1V5_S0_AUDIO_DIG	51
		=PP1V5_S0_PCH_VCCSUSHDA	8 11 17
77	PP1V05_S0 MAKE_BASE=TRUE	PP1V05_S0_REG	60
		=PP1V05_S0_PCH_VCC	8 11
		=PP1V05_S0_PCH_VCCASW	8 11
		=PP1V05_S0_PCH_VCCCLK	8 11
		=PP1V05_S0_PCH_VCCIO_USB2	8 11
		=PP1V05_S0_PCH_VCCHSIO	8 11
		=PP1V05_S0_PCH_VCCIO_HSIO	8
		=PP1V05_S0_PCH_PLLFILTERS	11
		=PP1V05_S0_SMC	44
		=PP1V05_S0_XDP	16
		=PP1V05_S0_CPU_VCCST	6 8 15 16 17 53
		=PP1V05_S0_PCH_VCCPLL_HSIO	11
78	PPCPUVCC_S0_CPU MAKE_BASE=TRUE	PPCPUVCC_S0_REG	59
		=PPCPUVCC_S0_CPU	47
		=PPVCC_S0_CPU	8 10

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Power Aliases

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PCH Miscellaneous

12 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_CAMERAP — NC_PCIE_CLK100M_CAMERAP
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_CAMERAN — NC_PCIE_CLK100M_CAMERAN
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_FWP — NC_PCIE_CLK100M_FWP
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_FWN — NC_PCIE_CLK100M_FWN
MAKE_BASE=TRUE NO_TEST=1

Unused Thunderbolt Aliases

26 TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=1

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Unused Signal Aliases

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Functional / ICT Test

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J70 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	0.145 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.092 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.150 MM	0.076 MM	=STANDARD	0.120 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.174 MM	0.085 MM	=STANDARD	0.120 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	Y	0.141 MM	0.076 MM	=STANDARD	0.130 MM	0.1 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.120 MM	0.076 MM	=STANDARD	0.140 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.108 MM	0.076 MM	=STANDARD	0.150 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.099 MM	0.076 MM	=STANDARD	0.170 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.175 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.076 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.085 MM	=STANDARD	0.210 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.070 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

_____	Top	Signal	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	2	Plane	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	3	Signal	0.5 OZ
_____		Prepreg	0.435 MM
_____	4	Plane	1 OZ
_____		Core	0.152 MM
_____	5	Plane	1 OZ
_____		Prepreg	0.435 MM
_____	6	Signal	0.5 OZ
_____		Prepreg	0.070 MM
_____	2	Plane	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	Btm	Signal	1/3 OZ (CU PLATED)

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J70 RULE DEFINITIONS

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
DDR_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_70D
DDR_CTRL_PHY	*	DDR_40S
DDR_CMD_PHY	*	DDR_40S
DDR_DQ_PHY	*	DDR_40S
DDR_DQS_PHY	*	DDR_70D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=4:1_SPACING	?
DDR_STROBE_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (HSW U/Y PDG, Intel Doc# 502636)

BDW does not have a separate power spec from HSW, so this document is still accurate

Table	Trace	Design	Iso	Design	Comments
6-14	4	(diff)	16	19.69	CLK trace spacing controlled by =70_OHM_DIFF.
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	16	11.81	DQ to other signals not in the same bytelane (but not ch)
			12	11.81	DQS to other signals of the same channel
			7.5	7.87	DQ to DQ in the same bytelane of the same channel
			12	11.81	DQ to DQS in the same bytelane of the same channel
			16	11.81	DQ or DQS in different bytelanes of the same channel
			?	25.59	DQ or DQS in different channels. ISO RULE NOT IN PDG
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_STROBE_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_STROBE_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
1178 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<0>	? 21 25
1179 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<0>	? 21 25
1258 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1>	? 22 25
1259 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1>	? 22 25
1262 DDR_A_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<0>	? 21 22 25
1181 DDR_A_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1>	? 21 22 25
1182 DDR_A_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<0>	? 21 22 25
1180 ?	?	?	MEM_A_CKE<1..0>	? 21 25
1247 ?	?	?	MEM_A_CKE<3..2>	? 22 25
1183 ?	?	?	MEM_A_CAA<9..0>	? 21 25
1184 ?	?	?	MEM_A_CAB<9..0>	? 22 25
1188 ?	?	?	MEM_A_DQ<7..0>	? 19
1189 ?	?	?	MEM_A_DQ<15..8>	? 19
1191 ?	?	?	MEM_A_DQ<23..16>	? 19
1190 ?	?	?	MEM_A_DQ<31..24>	? 19
1192 ?	?	?	MEM_A_DQ<39..32>	? 19
1193 ?	?	?	MEM_A_DQ<47..40>	? 19
1194 ?	?	?	MEM_A_DQ<55..48>	? 19
1195 ?	?	?	MEM_A_DQ<63..56>	? 19
1196 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	? 19
1197 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	? 19
1198 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	? 19
1199 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	? 19
1200 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	? 19
1201 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	? 19
1203 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	? 19
1202 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	? 19
1204 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	? 19
1205 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	? 19
1206 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	? 19
1207 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	? 19
1208 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	? 19
1209 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	? 19
1210 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	? 19
1211 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	? 19
Channel B				
1212 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<0>	? 23 25
1213 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<0>	? 23 25
1260 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1>	? 24 25
1261 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1>	? 24 25
1263 DDR_B_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<0>	? 23 24 25
1215 DDR_B_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1>	? 23 24 25
1216 DDR_B_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<0>	? 23 24 25
1214 ?	?	?	MEM_B_CKE<1..0>	? 23 25
1255 ?	?	?	MEM_B_CKE<3..2>	? 24 25
1217 ?	?	?	MEM_B_CAA<9..0>	? 23 25
1218 ?	?	?	MEM_B_CAB<9..0>	? 24 25
1222 ?	?	?	MEM_B_DQ<7..0>	? 19
1223 ?	?	?	MEM_B_DQ<15..8>	? 19
1225 ?	?	?	MEM_B_DQ<23..16>	? 19
1224 ?	?	?	MEM_B_DQ<31..24>	? 19
1226 ?	?	?	MEM_B_DQ<39..32>	? 19
1227 ?	?	?	MEM_B_DQ<47..40>	? 19
1228 ?	?	?	MEM_B_DQ<55..48>	? 19
1229 ?	?	?	MEM_B_DQ<63..56>	? 19
1230 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	? 19
1231 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	? 19
1232 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	? 19
1233 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	? 19
1234 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	? 19
1235 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	? 19
1237 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	? 19
1236 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	? 19
1238 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	? 19
1239 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	? 19
1240 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	? 19
1241 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	? 19
1242 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	? 19
1243 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	? 19
1244 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	? 19
1245 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	? 19
SM COMP				
1257	?	?	CPU_SM_RCOMP<0..2>	6

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DDR3 Constraints

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PCI Express

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?
CPU_ASYNC_ISO	*	=3:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

CPU ASYNCHRONOUS

Electrical Contraint Set		Physical	Spacing		
1573		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 43 44 57
1574		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
1575	PECI	CPU_ASYNC_PHY	CPU_ASYNC_MS	CPU_PECI	6 44
1576		CPU_ASYNC_PHY	CPU_ASYNC_MS	SMC_PECI_L	43 44
1578		CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 44
1577		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6
1583		CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	15 44
1581		CPU_ASYNC_PHY	CPU_ASYNC	CPU_VCCST_PWRGD	8 16 17
1584		CPU_ASYNC_PHY	CPU_ASYNC	XDP_CPU_VCCST_PWRGD	16
1585		CPU_ASYNC_PHY	CPU_ASYNC	PLT_RESET_L	13 15 16 18
1582	?	?	?	XDP_BPM_L<1..0>	6 16

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
CPU OPI Compensation				
1570	COMP_PCIE_PHY	COMP_PCIE	CPU_OPI_RCOMP	6
CPU eDP Compensation				
1571	COMP_PCIE_PHY	COMP_PCIE	MCP_EDP_RCOMP	5
1572	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP	6

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CPU CONSTRAINTS

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=5X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
H140 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	12 26
H141 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	12 26
H132 ?	?	?	PCIE_TBT_R2D_P<2..0>	26
H133 ?	?	?	PCIE_TBT_R2D_N<2..0>	26
H134	?	?	PCIE_TBT_R2D_C_P<2..0>	14 26
H135	?	?	PCIE_TBT_R2D_C_N<2..0>	14 26
H179 PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3>	26
H180 PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3>	26
H181	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3>	14 26
H182	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3>	14 26
H183 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<0>	14 26
H184 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<0>	14 26
H185	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<0>	26
H186	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<0>	26
H176 ?	?	?	PCIE_TBT_D2R_P<2..1>	14 26
H177 ?	?	?	PCIE_TBT_D2R_N<2..1>	14 26
H178	?	?	PCIE_TBT_D2R_C_P<2..1>	26
H179	?	?	PCIE_TBT_D2R_C_N<2..1>	26
H187 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3>	14 26
H188 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3>	14 26
H189	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3>	26
H190	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3>	26
x1 AirPort				
H142 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	31
H143 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	31
H144	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	14 31
H146	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	14 31
H145 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	14 31
H147 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	14 31
H148 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	12 31
H149 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	12 31
x1 Caesar IV				
H151 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	34
H150 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	34
H152	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	14 34
H154	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	14 34
H153 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	14 34
H155 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	14 34
H156	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	34
H157	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	34
H158 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	12 34
H159 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	12 34
x2 SSD				
H172 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	12 32
H173 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	12 32
PCH PCIE Compensation				
H178	COMP_PCIE_PHY	COMP_PCIE	PCH_PCIE_RCOMP	14

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PCH PCIe/DMI Constaints

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
192 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	33
192 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	33
188	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	12 33
188	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	12 33
191 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	12 33
191 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	12 33
187	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	33
187	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	33
PCH SATA Port 1 (SSD)				
192 ?	?	?	PCIE_SSD_R2D_P<0..1>	12 32
192 ?	?	?	PCIE_SSD_R2D_N<0..1>	12 32
1115 ?	?	?	SSD_R2D_C_P<0..1>	32
1116 ?	?	?	SSD_R2D_C_N<0..1>	32
1103 ?	?	?	PCIE_SSD_D2R_P<0..1>	12 32
1102 ?	?	?	PCIE_SSD_D2R_N<0..1>	12 32
PCH SATA Compensation				
1104	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	12

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
113 ?	?	?	XDP_BPM_L<7..2>	6 16
118 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<0>	6 16
1124 XDP_CPU_CFG1_PD	XDP_PHY	XDP	CPU_CFG<1>	6 16
1117 XDP_CPU_CFG	XDP_PHY	XDP	CPU_CFG<2>	6 16
1120 ?	XDP_PHY	XDP	CPU_CFG<3>	6 16
1119 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<4>	6 16
1121 ?	?	?	CPU_CFG<7..5>	6 16
1123 ?	?	?	CPU_CFG<10..8>	6 16
1122 ?	?	?	CPU_CFG<19..11>	6 16
145 XDP_CPU_TCK	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 16
146 XDP_CPU_TMS	XDP_PHY	XDP	XDP_CPU_TMS	6 16
147	XDP_PHY	XDP	XDP_CPU_TDI	6 16
148	XDP_PHY	XDP	XDP_CPU_TDO	6 16
119 XDP_CPU_TRST_L	XDP_PHY	XDP	XDP_CPU_TRST_L	6 16
PCH XDP				
149	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	12 16
150	XDP_PHY	XDP	XDP_PCH_TMS	12 16
151	XDP_PHY	XDP	XDP_PCH_TDI	12 16
152	XDP_PHY	XDP	XDP_PCH_TDO	12 16

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks.
					All signals default are 50 Ohm SE.

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SATA/FDI/XDP Constraints

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=4:1_SPACING	?
COMP_PCH_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
1336	?	?	LPC_AD<3..0>	14 43
1335	?	?	LPC_AD_R<3..0>	14
1338	LPC_55S	LPC	LPC_FRAME_L	14 43
1337	LPC_55S	LPC	LPC_FRAME_R_L	14
LPC Clocks				
1341	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC	17 43
1342	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC_R	12 17

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
1417	CLK_XTAL	XTAL	PCH_CLK24M_XTALIN	12 17
1418	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT	12 17
1419	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT_R	17
PCH RTC 32K				
1347	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	12 17
1348	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	12 17
1350	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	17
SMC 32K				
1349	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	13 44
1350	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	43 44

25 MHz XTALS

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
1379	CLK_XTAL	XTAL	TBT_CLK25M_IN	17 26
1380	CLK_XTAL	XTAL	TBT_CLK25M_OUT	17 26
1381	CLK_XTAL	XTAL	TBT_CLK25M_OUT_R	17
1384	CLK_XTAL	XTAL	ENET_XTAL_IN	17 34
1385	CLK_XTAL	XTAL	ENET_XTAL_OUT	17 34
1386	CLK_XTAL	XTAL	ENET_XTAL_OUT_R	17

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
1357 HDA_CLK	HDA	HDA	HDA_BIT_CLK	12 51
1361	HDA	HDA	HDA_BIT_CLK_R	12
1363 HDA_RST	HDA	HDA	HDA_RST_L	12 51
1362	HDA	HDA	HDA_RST_R_L	12
1364 HDA_OUT	HDA	HDA	HDA_SDOUT	12 51
1367	HDA	HDA	HDA_SDOUT_R	12 17
1366 HDA_SYNC	HDA	HDA	HDA_SYNC	12 51
1358	HDA	HDA	HDA_SYNC_R	12
1365 HDA_IN	HDA	HDA	HDA_SDIN0	12 51
SPDIF				
1370	HDA	HDA	DP_INT_SPDIF_AUDIO	39 51 80
1371	HDA_55S	?	SPDIF_OUT_JACK	51 54
1420	HDA_55S	?	CS4208_SPDIF_IN	51
1421	HDA_55S	?	CS4208_SPDIF_OUT	51

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
1391	SPI_50S	SPI	SPI_CLK_R	14 45
1392	SPI_50S	SPI	SPI_CLK	45
1393	SPI_50S	SPI	SPI_ALT_CLK	45
1408	SPI_50S	SPI	SPI_SMC_CLK	43 45
1407	SPI_50S	SPI	SPI_MLB_CLK	45
1394	SPI_50S	SPI	SPI_CS0_R_L	14 45
1395	SPI_50S	SPI	SPI_CS0_L	45
1396	SPI_50S	SPI	SPI_ALT_CS_L	45
1409	SPI_50S	SPI	SPI_SMC_CS_L	43 45
1397	SPI_50S	SPI	SPI_MLB_CS_L	45
1399	SPI_50S	SPI	SPI_MOSI_R	14 45
1400	SPI_50S	SPI	SPI_MOSI	45
1401	SPI_50S	SPI	SPI_ALT_MOSI	45
1410	SPI_50S	SPI	SPI_SMC_MOSI	43 45
1411	SPI_50S	SPI	SPI_MLB_MOSI	45
1404	SPI_50S	SPI	SPI_MISO	45
1403	SPI_50S	SPI	SPI_ALT_MISO	45
1412	SPI_50S	SPI	SPI_SMC_MISO	43 45
1413	SPI_50S	SPI	SPI_MLB_MISO	45
1405	SPI_50S	SPI	SPIROM_USE_MLB	15 45

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PCH and BR Constraints

Apple Inc.

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
1320 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_P	14 41
1321 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_N	14 41
1331	USB3_PHY	USB3	USB3_EXTA_D2R_F_P	41
1332	USB3_PHY	USB3	USB3_EXTA_D2R_F_N	41
1413 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_P	41
1414 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_N	41
1415	USB3_PHY	USB3	USB3_EXTA_R2D_F_P	41
1416	USB3_PHY	USB3	USB3_EXTA_R2D_F_N	41
1493	USB3_PHY	USB3	USB3_EXTA_R2D_CF_P	14 41
1494	USB3_PHY	USB3	USB3_EXTA_R2D_CF_N	14 41
1417 USB2_MUXED_MAJO_CONN	USB2_PHY	USB2	USB_EXTA_P	14 41
1418 USB2_MUXED_MAJO_CONN	USB2_PHY	USB2	USB_EXTA_N	14 41
1419	USB2_PHY	USB2	USB2_EXTA_MUXED_P	41
1420	USB2_PHY	USB2	USB2_EXTA_MUXED_N	41
1333	USB2_PHY	USB2	USB2_EXTA_P	41
1334	USB2_PHY	USB2	USB2_EXTA_N	41
External Port B (J4610)				
1421 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_P	14 41
1422 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_N	14 41
1423	USB3_PHY	USB3	USB3_EXTB_D2R_F_P	41
1424	USB3_PHY	USB3	USB3_EXTB_D2R_F_N	41
1425 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_P	41
1427 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_N	41
1428	USB3_PHY	USB3	USB3_EXTB_R2D_F_P	41
1429	USB3_PHY	USB3	USB3_EXTB_R2D_F_N	41
1495	USB3_PHY	USB3	USB3_EXTB_R2D_CF_P	14 41
1496	USB3_PHY	USB3	USB3_EXTB_R2D_CF_N	14 41
1430 USB2_CONN	USB2_PHY	USB2	USB_EXTB_P	14 41
1431 USB2_CONN	USB2_PHY	USB2	USB_EXTB_N	14 41
1432	USB2_PHY	USB2	USB2_EXTB_P	41
1433	USB2_PHY	USB2	USB2_EXTB_N	41
External Port C (J4700)				
1437 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_P	14 42
1439 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_N	14 42
1438	USB3_PHY	USB3	USB3_EXTC_D2R_F_P	42
1440	USB3_PHY	USB3	USB3_EXTC_D2R_F_N	42
1441 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_P	42
1442 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_N	42
1444	USB3_PHY	USB3	USB3_EXTC_R2D_F_P	42
1443	USB3_PHY	USB3	USB3_EXTC_R2D_F_N	42
1498	USB3_PHY	USB3	USB3_EXTC_R2D_CF_P	14 42
1497	USB3_PHY	USB3	USB3_EXTC_R2D_CF_N	14 42
1446 USB2_CONN	USB2_PHY	USB2	USB_EXTC_P	14 42
1445 USB2_CONN	USB2_PHY	USB2	USB_EXTC_N	14 42
1450	USB2_PHY	USB2	USB2_EXTC_P	42
1452	USB2_PHY	USB2	USB2_EXTC_N	42
External Port D (J4710)				
1453 USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_P	14 42
1455 USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_N	14 42
1454	USB3_PHY	USB3	USB3_EXTD_D2R_F_P	42
1456	USB3_PHY	USB3	USB3_EXTD_D2R_F_N	42
1457 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_P	42
1458 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_N	42
1460	USB3_PHY	USB3	USB3_EXTD_R2D_F_P	42
1459	USB3_PHY	USB3	USB3_EXTD_R2D_F_N	42
1499	USB3_PHY	USB3	USB3_EXTD_R2D_CF_P	14 42
1500	USB3_PHY	USB3	USB3_EXTD_R2D_CF_N	14 42
1462 USB2_CONN	USB2_PHY	USB2	USB_EXTD_P	14 42
1461 USB2_CONN	USB2_PHY	USB2	USB_EXTD_N	14 42
1468	USB2_PHY	USB2	USB2_EXTD_P	42
1469	USB2_PHY	USB2	USB2_EXTD_N	42
Camera (J3510)				
1374 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	14 37
1376 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	14 37
PCH USB Compensation				
1384	PCH_55S	COMP_PCH	PCH_USB_RBIAS	14

RMH Love

Electrical Contraint Set	Physical	Spacing		
1409 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	14 31
1410 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	14 31
1505 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	31
1506 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	31

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
1474 ?	?	?	ENETCONN_MDI_P<3..0>	34 35
1475 ?	?	?	ENETCONN_MDI_N<3..0>	34 35
1476	?	?	ENETCONN_MDI_T_P<3..0>	35
1477	?	?	ENETCONN_MDI_T_N<3..0>	35
1519		ENET_TRANS	ENETCONN_MCT0	35
1520		ENET_TRANS	ENETCONN_MCT1	35
1521		ENET_TRANS	ENETCONN_MCT2	35
1522		ENET_TRANS	ENETCONN_MCT3	35
1523		ENET_TRANS	ENETCONN_MCT_BS	35
1478	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	34
SD				
1479 ?	?	?	ENET_CR_DATA<7..0>	34
1480	?	?	SDCONN_DATA<7..0>	34 36
1481 SD_CMD	SD_PHY	SD	ENET_SD_CMD	34
1482	SD_PHY	SD	SDCONN_CMD	34 36
1483 SD_CLK	SD_PHY	SD	ENET_SD_CLK	34
1484	SD_PHY	SD	SDCONN_CLK	34 36
1486	SD_PHY	SD	SDCONN_CLK_R	36
1485	SD_PHY	SD	ENET_MEDIA_SENSE	15 34
1488	SD_PHY	SD	ENET_SD_DETECT_L	34 36
CIV SPI				
1490	CIV_SPI	SPI	ENET_SCLK	34
1489	CIV_SPI	SPI	ENET_MISO	34
1492	CIV_SPI	SPI	ENET_MOSI	34
1491	CIV_SPI	SPI	ENET_CS_L	34

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
1501 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	37
1502 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	37
1504 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	37
1503 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	37
1507	SPI_50S	SPI	CAM_SF_CLK	37
1508	SPI_50S	SPI	CAM_SF_CLK_R	37
1509	SPI_50S	SPI	CAM_SF_DIN	37
1510	SPI_50S	SPI	CAM_SF_DIN_R	37
1511	SPI_50S	SPI	CAM_SF_CS_L	37
1513	SPI_50S	SPI	CAM_SF_WP_L	37
1512	SPI_50S	SPI	CAM_SF_DOUT	37
1514	SPI_50S	SPI	CAM_SF_DOUT_R	37
1517	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	37
1518	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	37

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USB/Ethernet/SD Constraints

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set		Physical	Spacing		
Common					
E3			SENSE	GND_SMC_AVSS	43 44 47
12V S5 (System Total)					
E4	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	47
E5	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	47
E6			SENSE	ISNS_P12VG3H_R	47
E7			SENSE	ISNS_P12VG3H	44 47
E8			SENSE	VSNS_P12VG3H	44 47
SSD					
E85	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	47
E87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	47
E86			?	ISNS_SSDS4_R	47
E88			?	ISNS_SSDS4	44 47
E89			SENSE	VSNS_P3V3_SSD	44 47
VDDQ S3 (DDR)					
E33	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_P	47
E32	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_N	47
E35			SENSE	ISNS_P1V2_S3_DDR_R	47
E34			SENSE	ISNS_P1V2_S3_DDR	44 47
E36			SENSE	VSNS_P1V2_S3_DDR	44 47
CPU Core					
E42			SENSE	CPUVR_IMON	47 57
E45			SENSE	ISNS_CPUVCC	44 47
E46			SENSE	VSNS_CPUVCC	44 47

SMC

Electrical Contraint Set		Physical	Spacing		
SMC					
E1		CLK_XTAL	XTAL	SMC_XTAL	43 44
E2		CLK_XTAL	XTAL	SMC_EXTAL	43 44
E191		SMC_GEN	SMC_CTRL	SMC_LRESET_L	18 43
E90		SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	13 43
E92		SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	15 43
E93		SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	43 49
E94		SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	43 49

SMBus

Electrical Contraint Set		Physical	Spacing		
SMC					
E10		SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	43 46
E9		SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	43 46
E11		SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	43 46
E12		SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	43 46
E13		SMB_PHY	SMB	SMBUS_SMC_2_S0_SCL	43 46
E14		SMB_PHY	SMB	SMBUS_SMC_2_S0_SDA	43 46
E15		SMB_PHY	SMB	SMBUS_SMC_3_SCL	43 46
E16		SMB_PHY	SMB	SMBUS_SMC_3_SDA	43 46
E19		SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	43 44
E20		SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	43 44
PCH					
E21		TBT_I2C_5S8	TBT_I2C	SMBUS_PCH_CLK	14 46
E52		TBT_I2C_5S8	TBT_I2C	SMBUS_PCH_DATA	14 46
E53		SMB_PHY	SMB	SML_PCH_0_CLK	14 46
E54		SMB_PHY	SMB	SML_PCH_0_DATA	14 46

Temperature Sense

Electrical Contraint Set		Physical	Spacing		
EMC1414-1 (Production)					
E57	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	48
E58	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	48
E59	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_P	48
E60	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_N	48
E65	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	48 56
E66	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	48 56
E122		SNS_DIFF_PHY	SENSE	SNS_T1_2_P	48
E124		SNS_DIFF_PHY	SENSE	SNS_T1_2_N	48
TMP423 (Development)					
E67	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	48
E68	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	48
E69	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	48
E70	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	48
E71	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	48
E72	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	48
HDD Out-of-Band					
E73			SENSE	HDD_OOB1_D2R_L	33
E74			SENSE	HDD_OOB1_D2R_F_L	33
E75			SENSE	HDD_OOB1_D2R_R_L	33
E113			SENSE	SMC_OOB1_D2R_L	33 43
E76			SENSE	SMC_OOB1_R2D_L	33 43
E116			SENSE	SMC_OOB1_R2D_R_L	33
SSD Out-of-Band					
E77			SENSE	SMC_OOB2_R2D_L	32 44
E78			SENSE	SMC_OOB2_D2R_L	32 44

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ (1.2V)/VTT (0.6V) S3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I43 POWER	POWER	POWER	5V			PP5V_REG_P1V2_V5IN	59 77
Local Ground							
I44 GND	GND	GND	0V			AGND_P1V2_S3	59 77
VDDQ S3							
I45 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_PHASE_P1V2_S3	59
I47 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_PHASE_P1V2_S3_L	59
I46 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_BOOT_P1V2_S3	59
I48 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_BOOT_P1V2_S3_RC	59
I49 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_UGATE_P1V2_S3	59
I52 VR_DIDT_PHY	VR_SWITCH		TRUE			REG_LGATE_P1V2_S3	59
I51 VR_DIDT_PHY	VR_SWITCH	12V	TRUE			REG_SNUBBER_P1V2_S3	59
I53 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_VDDQSNS	59
I55 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_VREF	59
I54 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_REFIN	59
I57 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_MODE	59
I58 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_TRIP	59
I59 VR_CTL_PHY	VR_CTL					LDO_DDRVTTS0_SNS	59
I61 VR_CTL_PHY	VR_CTL					REG_P1V2_S3_VTTREF	59
Output Bus							
I60 POWER	POWER	POWER	1.2V			PP1V2_S3	66
I62 POWER_DDR	POWER_DDR	POWER_DDR	0.6V			PP0V6_S3_DDRVTT	66
Sensed							
I64 POWER	POWER	POWER	1.2V			PP1V2_S3_DDR	66

PCH 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I1	POWER	POWER	5V			REG_VCC_U7400	60
I2	POWER	POWER	5V			REG_PVCC_U7400	60
Local Ground							
I3	GND	GND	0V			AGND_P1V05S0	60
1.05V S0							
I5	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	60
I4	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	60
I7	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	60
I6	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0_RC	60
I8	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	60
I9	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	60
I10	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	60
I12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	60
I11	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	60
I14	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	60
I86 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P1V05S0_PHASE_SNS_P	60
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P1V05S0_PHASE_SNS_M	60
I19		SENSE				REG_P1V05S0_FB	60
I18		SENSE				REG_P1V05S0_RTN	60
I21	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	60
I20	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	60
Output Bus							
I22	POWER	POWER	1.05V			PP1V05_S0	66

1.8V S3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I67 POWER	POWER	POWER	5V			PP5V_REG_P1V2_V5IN	59 77
Local Ground							
I68 GND	GND	GND	0V			AGND_P1V2_S3	59 77
Switch							
I69 VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE			REG_SW_P1V8_S3	59
I70 VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE			REG_FB_P1V8_S3	59
Output Bus							
I83 POWER	POWER	1.8V				PP1V8_S3_REG_R	59
I84 POWER	POWER	1.8V				PP1V8_S3	66

1.05V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
Switch							
Output Bus							
I92			1.05V			PP1V05_S5	16

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
R124	POWER	POWER	12V			PP12V_S0_REG_CPUVCC_VIN	57
R137	POWER	POWER	5V			PP5V_S0_REG_CPUVCC_VDD	57
Phase 1							
R884	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1	57 58
R887	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1	58
R888	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1	58
R890	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1_RC	58
R127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1	58
R126	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1	58
R892	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1	58
R893	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1	58
R894 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS1_M	58
R895 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS1_P	58
R896		SENSE				REG_CPUVCC_ISEN1	57 58
R127		SENSE				REG_CPUVCC_ISUMN	57 58
R127		SENSE				REG_CPUVCC_ISUMP	57 58
Phase 2							
R114	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2	57 58
R114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2	58
R114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2	58
R114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2_RC	58
R127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2	58
R127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2	58
R114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2	58
R114	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2	58
R114 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS2_M	58
R115 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_CPUVCC_ISNS2_P	58
R115		SENSE				REG_CPUVCC_ISEN2	57 58

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
ISL95826HRZ							
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FCCM	57 58
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DRSEL	57
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP	57
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP_RC	57
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB	57
R102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB_RC	57
R103	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB2	57
R103 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P	8 57
R104 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N	9 57
R103		SENSE				CPU_VCCSENSE_P_R	57
R103		SENSE				CPU_VCCSENSE_P_RC	57
R103		SENSE				REG_CPUVCC_ISUMN_RC	57
R103		SENSE				REG_CPUVCC_ISUMN_R	57
R103		SENSE				REG_CPUVCC_RTN	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC_R	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_SLOPE	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG1	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG2	57
R105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG3	57
R106 CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK	8 57
R106	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	8
R106 CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	8 57
R106	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	8
R106 CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT	8 57
R106	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	8
Output Bus							
R104	POWER	POWER	1.8V			PPCPUVCC_S0_CPU	44

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12V

Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus						
81449 POWER	POWER	12V			PP12V_ACDC	66
FET Switched						
81448 POWER	POWER	12V			PP12V_S5	66
81453 POWER	POWER	12V			PP12V_S0	66
Sensed						
81452 POWER	POWER	12V			PP12V_G3H	66

3.42V G3H

Physical	Spacing	Voltage	DIDT	NO_TEST		
3.42V G3H						
81443 POWER	POWER	12V	TRUE		P3V42G3H_BOOST	56
81442 POWER	POWER	12V	TRUE		P3V42G3H_SW	56
81444 VR_CTL_PHY	VR_CTL				P3V42G3H_FB	56
81445 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	56
81485 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_R_L	56
Output Bus						
81446 POWER	POWER	3.425V			PP3V42_G3H	66
81484 POWER	POWER	3.425V			PP3V42_G3H_REG_R	56

3.3V G3

Physical	Spacing	Voltage	DIDT	NO_TEST		
81476 POWER	POWER	3.3V			PP3V3_G3	66

3.3V S5/5V S4

Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus						
81843 POWER	POWER	12V			REG_VIN_U7600	61
81255 POWER	POWER	5V			REG_VCC1_U7600	61
81255 POWER	POWER	5V			REG_VCC2_U7600	61
3.3V S5						
81849 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	61
81847 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	61
81851 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5_RC	61
81848 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	61
81850 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5	61
81852 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	61
81107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	61
81072 VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	61
81130 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	61
81108 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	61
81075 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	61
81107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	61
5V S4						
81139 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	61
81138 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	61
81137 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4_RC	61
81140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	61
81141 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4	61
81142 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	61
81146 VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	61
81145 VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	61
81143 VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	61
81146 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	61
81145 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	61
81146 VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	61
Output Bus						
81153 POWER	POWER	5V			PP5V_S5	66
81153 POWER	POWER	5V			PP5V_S4	66
81149 POWER	POWER	3.3V			PP3V3_S5	66
FET Switched						
81230 POWER	POWER	5V			PP5V_S0	66
81210 POWER	POWER	3.3V			PP3V3_S4	66
81233 POWER	POWER	3.3V			PP3V3_S0	66
81452 ?	?	3.3V			PP3V3_S4_SSD	66
81210 POWER	POWER	3.3V			PP3V3_ENET	66
81180 POWER	POWER	3.3V			PP3V3_TBTLC	18 26 27
Sensed						
81452 ?	?	3.3V			PPSSD_S4	66

HDD S0

Physical	Spacing	Voltage	DIDT	NO_TEST		
FET Switched						
81160 POWER	POWER	5V			PP5V_S0_HDD	66

1V5 S0

Physical	Spacing	Voltage	DIDT	NO_TEST		
OUTPUT BUS						
81157 POWER	POWER	1.5V			PP1V5_S0	66

Ground/Common

Physical	Spacing	Voltage	DIDT	NO_TEST		
Common						
GND	GND				GND\G	
81180 GND	GND	0V			PGND_REG_P1V2_S3	59

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
81500 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P3V3S5_PHASE_SNS_P	61
81500 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P3V3S5_PHASE_SNS_M	61
81500 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P5VS4_PHASE_SNS_P	61
81500 SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P5VS4_PHASE_SNS_M	61

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP	*	*	TBTDP_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBT_I2C	*	*	TBT_I2C_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

	Electrical Contraint Set	Physical	Spacing		
1511		?	?	DP_TBTSNK0_ML_C_P<3..0>	5 26
1512		?	?	DP_TBTSNK0_ML_C_N<3..0>	5 26
1513	?	?	?	DP_TBTSNK0_ML_P<3..0>	26
1514	?	?	?	DP_TBTSNK0_ML_N<3..0>	26
1516		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	13 26
1515		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	13 26
1517	DP_TBTSNX0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	26
1518	DP_TBTSNX0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	26
1519		?	?	DP_TBTSNK1_ML_C_P<3..0>	5 26
1521		?	?	DP_TBTSNK1_ML_C_N<3..0>	5 26
1520	?	?	?	DP_TBTSNK1_ML_P<3..0>	26
1523	?	?	?	DP_TBTSNK1_ML_N<3..0>	26
1522		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	13 26
1524		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	13 26
1526	DP_TBTSNX1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	26
1525	DP_TBTSNX1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	26
1603	?	?	?	DP_TBTSRC_ML_P<1..0>	26 40
1604	?	?	?	DP_TBTSRC_ML_N<1..0>	26 40
1606	?	?	?	DP_TBTSRC_ML_C_P<1..0>	
1607	?	?	?	DP_TBTSRC_ML_C_N<1..0>	
1529	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_P	26 40
1530	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_N	26 40
1601		?	?	DP_TBTSRC_AUX_C_P	
1602		?	?	DP_TBTSRC_AUX_C_N	
1532	TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	26
1531	TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	26
1533	TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	26
1535	TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	26

*: Only used on hosts supporting T29 video-in

DisplayPort

	Electrical Contraint Set	Physical	Spacing		
	Graphics Source				
1642	?	?	?	DP_INT_ML_P<1..0>	5 40
1643	?	?	?	DP_INT_ML_N<1..0>	5 40
1644	DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	5 40
1645	DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	5 40
1646		?	?	DP_INT_AUX_C_P	
1647		?	?	DP_INT_AUX_C_N	
	Internal Panel				
1605		?	?	DP_INTPNL_ML_C_P<1..0>	40
1608		?	?	DP_INTPNL_ML_C_N<1..0>	40
1607	?	?	?	DP_INTPNL_ML_P<1..0>	39 40
1608	?	?	?	DP_INTPNL_ML_N<1..0>	39 40
1609	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	39 40
1610	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	39 40
	Internal DP SPDIF				
1611			HDA	DP_INT_SPDIF_AUDIO	39 51 74
	DDC				
1692		TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_CLK	13 30
1693		TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_DATA	13 30
1694		TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_CLK	13 30
1695		TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_DATA	13 30
1698		TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	28 30
1699		TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	28 30
1697		TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	29 30
1696		TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	29 30

TBT/DP Net Properties

	Electrical Contraint Set	Physical	Spacing		
	Port A				
1541	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	26 28
1542	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	26 28
1544		TBTDP_90D	TBTDP	TBT_A_R2D_P<1>	28
1543		TBTDP_90D	TBTDP	TBT_A_R2D_N<1>	28
1700	TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	26 28
1701	TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	26 28
1702		TBTDP_90D	TBTDP	TBT_A_R2D_P<0>	28
1703		TBTDP_90D	TBTDP	TBT_A_R2D_N<0>	28
1535	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	26 28
1536	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	26 28
1545		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	28
1547		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	28
1680	DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	26 28
1681	DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	26 28
1678		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	28
1679		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	28
1516	DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	28
1518	DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	28
1554	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	26 28
1553	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	26 28
1711		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1>	28
1710		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1>	28
1675	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	26 28
1674	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	26 28
1649		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<0>	28
1650		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<0>	28
1650	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	28
1651	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	28
1599	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	26 28
1600	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	26 28
1555		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	28
1556		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	28
	Port B				
1652	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	26 29
1653	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	26 29
1655		TBTDP_90D	TBTDP	TBT_B_R2D_P<1>	29
1654		TBTDP_90D	TBTDP	TBT_B_R2D_N<1>	29
1704	TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	26 29
1705	TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	26 29
1707		TBTDP_90D	TBTDP	TBT_B_R2D_P<0>	29
1706		TBTDP_90D	TBTDP	TBT_B_R2D_N<0>	29
1657	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	26 29
1658	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	26 29
1683		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	29
1682		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	29
1685	DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	26 29
1684	DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	26 29
1656		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	29
1660		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	29
1659	DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	29
1662	DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	29
1665	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	26 29
1664	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	26 29
1708		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1>	29
1709		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1>	29
1676	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	26 29
1677	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	26 29
1681		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<0>	29
1683		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<0>	29
1671	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	29
1673	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	29
1666	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	26 29
1667	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	26 29
1669		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	29
1670		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	29

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TBT/DP Constraints

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
J822	POWER	POWER	12V			PP12V_BKLT_SNS	62
J823	POWER	POWER	12V			PP12V_BKLT_FUSED	62
J750	POWER	POWER	12V			PP12V_S0_BKLT_FILT	62
J772	POWER	POWER	12V			PP12V_S0_BKLT_PWR	62
J774	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R	62
J775	POWER	POWER	5V			PP5V_S0_BKLT_R	62
J776	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R	62
Local Ground							
J831	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT	62
J829	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT	62
J830	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT	62
Backlight							
J752	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE	62
J753	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE	62
J754	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R	62
J755	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_SNUBBER	62
J757	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R	62
J759	BLC_CTL_PHY	BLC_CTL				BKLT_ISET	62
J763	BLC_CTL_PHY	BLC_CTL				BKLT_FLT	62
J765	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC	62
J797	SNS_DIFF_PHY	SENSE				BKLT_SW_P	62
J798	SNS_DIFF_PHY	SENSE				BKLT_SW_M	62
J762		SENSE				BKLT_FB	62
J821		BLC_HV	67V			BKLT_FB_XW	62
J824		BLC_HV	67V			BKLT_FB_R	62
J766	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1	62
J767	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2	62
J768	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3	62
J769	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4	62
J770	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5	62
J771	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6	62
J789	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R	62
J788	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R	62
J790	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R	62
J791	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R	62
J792	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R	62
J793	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R	62
J783	POWER_BLC_RET	BLC_HV				LED_RETURN_1	62
J782	POWER_BLC_RET	BLC_HV				LED_RETURN_2	62
J784	POWER_BLC_RET	BLC_HV				LED_RETURN_3	62
J785	POWER_BLC_RET	BLC_HV				LED_RETURN_4	62
J786	POWER_BLC_RET	BLC_HV				LED_RETURN_5	62
J787	POWER_BLC_RET	BLC_HV				LED_RETURN_6	62
Output Bus							
J770	POWER_BLC	BLC_HV	67V			BKLT_BOOST	62
J773	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1	62
J774	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2	62

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing		
SPI				
J544	SMB_PHY	SMB	BKLT_SCL	62
J543	SMB_PHY	SMB	BKLT_SDA	62

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BLC Constraints

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